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SERVICE INFORMATION

JOHN FLUKE MFG. CO., INC.

MONTRONICS, INC.
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TECHNICAL DATA FILE

JOHN FLUKE MFG. CO., INC. ■ MODEL **8100A**

FLUKE

DIGITAL MULTIMETER

FEATURES:

- *"RECIRCULATING REMAINDER" * A/D CONVERSION*
- *INTERNAL BATTERY OPERATION OPTIONAL*
- *COMPLETE MULTIMETER*
- *FOUR DIGITS PLUS OVERRANGE*

APPLICATIONS:

- *MEASURE AC AND DC TO 1200 VOLTS*
- *MEASURE RESISTANCE TO 12 MEGOHMS*
- *COMPLETE PORTABILITY WITH BATTERY OPTION*
- *FULLY ISOLATED MEASUREMENTS*

* Patent Pending

DESCRIPTION

Model 8100A is a compact, lightweight digital multimeter displaying four full decades plus a "1" for 20% overrange. It may be operated from line power or optional self-contained rechargeable batteries. AC volts, DC volts and kilohms are standard functions, selection being made via pushbutton switches. A switched 2-pole active filter and instantaneous, automatic polarity selection and display are additional standard features.

Analog inputs to the 8100A are processed through a buffer amplifier, the output of which is periodically sampled by a unique, Fluke designed, "Recirculating Remainder" analog-to-digital converter. The converter uses only one BCD counter and resistive ladder network to serially determine and display all digits. A unique capacitor register is used to hold the digits of the sample for continuous display between samples. Necessary converter switching is accomplished with field-effect transistors.

The analog circuitry also makes multiple use of scaling resistors and passive components. The combined analog and digital circuitry has low power consumption and a low total parts count, which leads to high reliability and optional battery operation.

High quality wire-wound resistors, polystyrene capacitors and an extremely stable reference amplifier are used in conjunction with the buffer amplifier and a high accuracy comparator to ensure precise, stable, digitizing of the analog input.

Custom packaging of the 8100A combines an attractive appearance with rugged construction. A single fiberglass circuit board is solidly secured to its strong aluminum chassis. Guard shields surround all critical analog and digital circuitry. Tough, scuff resistant plastic covers provide exterior protection. An accessory cover is available to protect the front panel during transit. A locking tilt-up bail is also used as a carrying handle. The line cord is detachable. A concealed slide switch at the rear of the instrument is used for selection of 115V or 230V AC line power.

The optional, rechargeable battery pack may be installed in the field or factory. A meter along side the digit readout is provided to indicate the state of battery charge. The battery is automatically charged when the 8100A is operated from line power. Disconnecting the line cord enables battery operation.

SPECIFICATIONS

DC VOLTS

Ranges	±1V, ±10V, ±100V and ±1000V 20% overrange on all ranges.
Resolution	0.01% of range. (100 uv on 1V range maximum)
Accuracy	
30 days, 20°C to 30°C	±(0.02% of input + 0.01% of range)
90 days, 15°C to 35°C	±(0.05% of input + 0.01% or range)
DC Input Resistance	Constant 10 megohms on all ranges.
Filter	Switch selected 2-pole, linear phase active filter.
Response Time to Rated Accuracy (max.)	0.5 seconds with filter out. 1.5 seconds with filter in.

SPECIFICATIONS *(Continued)*

Rejection . . . . . .

		INTERFERENCE FREQUENCY			
		60 Hz		50 Hz	
	DC	FILTER IN	FILTER OUT	FILTER IN	FILTER OUT
COMMON MODE (1K in Low Lead)	120 db	120 db	100 db	120 db	100 db
NORMAL MODE	----	60 db	20 db	47 db	9 db

NOTE: Common Mode Rejection approaches infinity when instrument is battery operated.

Polarity . . . . . Automatic, instantaneous selection and display.

Overload . . . . . ±1200 VDC or ±1700V peak AC can be applied continuously to any range without damage.

AC VOLTS

Ranges . . . . . 1V, 10V, 100V and 1000V. 20% overrange on all ranges.

Resolution . . . . . 0.01% of range. (100 uv on 1V range maximum)

Accuracy . . . . . MIDBAND 50 Hz - 10 kHz; EXTENDED 30 - 50 Hz and 10 - 20 kHz

90 days, 15°C to 35°C: ±(0.2% of input + 0.05% of range) ; ±(0.5% of input + 0.1% of range)

Input Impedance . . . . . 1 megohm shunted by < 30 pf.

Response Time to Rated Accuracy . . . . . 3 seconds.

Maximum DC Normal Mode Voltage . . . . . ±1200 VDC NOTE: The sum of DC Normal Mode Voltage and peak AC voltage must not exceed ±1700V.

Overload . . . . . ±1200 VDC or ±1700V peak AC from 30 Hz to 20 kHz can be applied continuously to any range without damage.

RESISTANCE

Ranges . . . . . 1K, 10K, 100K, 1000K and 10M. (20% overrange on all ranges)

Resolution . . . . . 0.01% of range (0.1 ohm on 1K range maximum)

Accuracy . . . . . 1K - 1000K ; 10M

30 days, 20°C to 30°C: ±(0.05% of input + 0.01% of range) ; ±(0.1% of input + 0.01% of range)

90 days, 15°C to 35°C: ±(0.1% of input + 0.02% of range) on all ranges

Configuration . . . . . Two terminal, constant current.

Voltage Across Input . . . . . 1.0V at full range.
1.2V at 20% overrange.
9V with open terminals.

Power In Unknown R . . . . . ⩽ 1 milliwatt in range and ⩽ 1.44 milliwatts at 20% overrange on the 1K range, decreasing by an order of magnitude per range to 100 nanowatts at 10 megohms.

Response Time to Rated Accuracy	1K - 1000K	10M
Filter Out	0.5 seconds	3.0 seconds
Filter In	2.0 seconds	10.0 seconds

Overload

1K Range . . . . . 130V RMS may be applied continuously without damage.

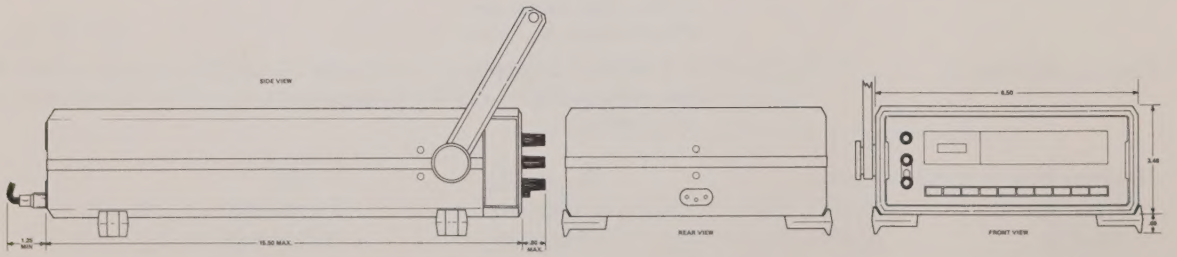
1K - 10M . . . . . 230V RMS may be applied continuously without damage.

SPECIFICATIONS *(Continued)*

GENERAL

Selection	Manual via mechanically interlocked pushbuttons.
Display	Four decade neon in-line readout with polarity neon for DC volts and fifth digit for 20% overrange. Automatic decimal location.
Sample Rate	3 samples per second.
Maximum Inputs	
"HI" to "LO"	See "Overload" specification by function.
"LO" to "Guard"	100V DC or peak AC.
"Guard" to "Chassis"	1200V DC or 230V RMS at 60 Hz.
Power	8 watts from 115V/230V, ±10%, 50-500 Hz line with internal battery option –01. 8 hours continuous operation from the rechargeable nickel-cadmium batteries.
Weight	8 pounds without batteries. 10 pounds with batteries.
Storage Temperature	–40°C to +75°C. (–40°C to +60°C with batteries)
Operating Temperature	0°C to +50°C.
Temperature Coefficient (outside limits shown in 30 and 90 day specifications)	DC ±(0.0025% of input +0.001% of range)/°C AC ±(0.015% of input +0.005% of range)/°C KΩ ±(0.0035% of input +0.0015% of range)/°C 10 MΩ ±(0.01% of input +0.002% of range)/°C
Humidity Range	80% R.H. max. at temp. ⩽ 35°C; 70% R.H. max from 35°C to 50°C.
Shock and Vibration	Meets requirements of MIL-T-21200G and MIL-E-16400F.
Mounting	Tilt down carrying handle detents into custom non-marring feet and serves as a tilt-up bail for bench use.

Price:	Model 8100A	$695 (without battery)
	Model 8100A-01	$795 (factory installed battery option)
	8100A-01 Kit	$100 (for field installation of battery option)
Accessories:	80-RF	$100 (R.F. Probe, 500 MHz)
	80F-5	$150 (High Voltage Probe, 5 kv)
	80F-15	$175 (High Voltage Probe, 15 kv)
	A-90	$255 (6 Range AC/DC Current Shunt to 10A)
	MEE-4008	$10.00 (Front Panel Dust Cover)
	MEE-7006	$40.00 (Rack Mtg. Ears -- Single Unit, Center Mount)
	MEE-7013	$40.00 (Rack Mtg. Ears -- Single Unit, Right or Left Offset)
	MEE-7014	$25.00 (Rack Mtg. Kit -- Two Units , Side-by-Side)



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8100A DIGITAL MULTIMETER OPERATIONAL THEORY

The 8100A consists of three main sections, referring to Figure 1 and the Schematic Drawings.

1. The Buffer section acts as a signal conditioner, capable of dividing voltage inputs, filtering and impedance conversion. The input divider also functions as a portion of the current source in the resistance ranges. (See Figure 2)
2. The Analog/Digital Conversion system, accepts the output from the Buffer and digitizes it using FLUKE'S Recirculating Remainder system of conversion. The unit samples three times a minute and recycles every 20 milliseconds.
3. The display section accepts the BCD output of the Analog to Digital Converter and puts it into ten line decimal output and displays the result on NIXIE tubes on a timed pulse basis.

In addition to the three main sections described above, the Power Supply serves dual functions. In addition to supplying the voltages required by the instrument it also contains an inverter that is used to both produce operating voltages for the instrument and supplies the clock or synchronization for timing the instrument.

Power for the 8100A is supplied by either the AC power line or via the internal battery pack, as furnished with the -01 option. When operated from line voltage transformer T101 provides two outputs. One output is rectified and filtered and used for the −18 volt supply in the instrument. The other winding provides a higher voltage which is rectified and used to charge the battery option, through DS11 which acts as a series limiting element.

The voltage supplied by the line voltage conversion is always greater than the voltage from the batteries, back biasing CR34 which prevents draining the batteries. The negative voltage, from either the batteries or the rectifiers CR1 and CR2, is regulated and filtered after passing through the protective fuse F2 and then on to supply the instrument all of it's negative voltage needs.

The −18 volts operates a 250 Hz inverter consisting of Q4, Q5 and a driver transformer T102. The output voltages from T102 are then conditioned to supply the remaining potential needs of the 8100A.

A high voltage winding (100v) operates a doubler rectifier circuit which provides 200v DC which is pulsed on every 4 milliseconds for 2 milliseconds. This provides a pulse for the last half of each time period of the instrument. This +200v DC is used to pulse the readout tubes.

T102 also provides one output which is rectified and filtered to +5 volts which is used to supply all of the integrated circuit logic. Another winding of T102 provides a voltage which is rectified and regulated to provide the +15 volts needed as a positive supply in the instrument. This +15 volts is further dropped by a zener regulated circuit to provide the +7.0 volt reference needed in the 8100A. This +7.0 volt reference supply has a fixed load of 2 ma in R181 and is protected from current reversals when an overload occurs in the ohms configuration by CR10.

INPUT RANGE DIVIDER (Figure 2)

The function switching on the front panel will provide one of the four basic configurations shown in Figure 2. When the instrument is operated in the DC volts position the divider will provide divisions of 1, 10, 100 and 1000 in order to maintain a 1 volt in put into the Buffer. The input divider consists of R158, R159, R160 and R156, R157 is provided for calibration.

In the K Ohms function, the bottom of the input divider (R160) is removed from the common binding post and connected to the +7.0 volt reference supply. The divider now acts as the current supply for resistance measurements.

In the 10M Ohm function the bottom end of the range divider is connected to divider R152 and R154 which can be adjusted by R153 to provide 10M Ohm calibration.

When the AC Volts function is selected the input configuration is changed to an operational rectifier. A pair of rectifier diodes is placed inside a strong feedback loop. A negative feedback signal proportional to the input voltage is developed across R161, R162, R174 and calibration pot R34, which is fed to the A-D Amplifier.

INPUT FILTER

The output of the Range Divider is fed into a two pole, active filter consisting of R27, R28, C10, C11, C12 and C13. (Filter switch out.) The settling time is .25 sec and 60 Hz is attenuated about 20 db. With the Filter switch depressed, C10 and C13 are removed from the circuit and the settling time becomes 1 second and 60 Hz is now attenuated about 60 db. CR11 and CR12, together with R27 provide protection for both the filter and the Buffer amplifier from excessive voltage inputs. In the 10 volt range, R27 is switched out since the output impedance of the range divider is 1M Ohm and R27 is not needed.

BUFFER AMPLIFIER

Q77 is a low noise, low drive J-FET pair, operating in a common source configuration and serves as the input stage to the Buffer Amplifier configuration. R175 is the zero adjustment pot, which in conjunction with R176, R177 and R188 forms a network by which the initial offset of Q77 can be reduced to zero. The output of Q77 drives A1, a monolithic operational amplifier, which provides the bulk of the gain. C51 is placed around A1 to provide a smooth roll off through unity gain. Q79 is a common base output stage whose purpose is to raise the output impedance of the amplifier as high as possible. In order to avoid degrading the high output impedance, Q79 operates into a constant load current, Q80. The Buffer amplifier feedback loop is completed through diodes CR14 and CR15, which provide a voltage step around zero to drive the following polarity sensing circuit. R174 provides the load resistance for the amplifier.

When AC Volts function is selected, the buffer amplifier is connected as an operational rectifier with R24 as the input resistor, AC coupled through C9 and R29, R30, R31 and R32 as the negative feedback ranging resistors. Diodes CR14 and CR15 now act as an operational rectifier. The positive half cycles only flow through CR15 and R162 where they develop a half wave rectified DC voltage proportional to the average value of the AC input. The high output impedance of Q79 and Q80 aids appreciably in improving the linearity at low levels where the threshold voltages of CR14 and CR15 tend to lower the amplifier loop gain. The half wave rectifier output is smoothed by two stage RC filter R35, C19, R36 and C20 to provide a 1 volt full scale output for the A-D Converter. Because the input capacity of Q77, along with additional stray capacities, causes an additional pole in the loop response of the AC converter. Trimmer capacitors C14 and C15 are provided on the two lowest ranges to adjust the frequency response up through 20 kHz. The low resistances of R31 and R32 make this unnecessary on the two upper ranges.

A-D CONVERTER (Figure 1)

The A-D Converter is synchronously operated. That is to say; it progresses through it's steps in time with an internal clock, which is the Power Supply Inverter (250 Hz). A Ring Counter fed by one of the outputs of T102, divides each cycle into five time periods of 4 milliseconds each. The first time period is the ZERO time, this is the time period when the offset is removed from the A-D Converter amplifier. During the remianing four time periods each of the four digits is digitized and then displayed. At the end of the last period, the Ring Counter supplies a synchronizing pulse through R68, C27, R69 and C28 to the Measure Store Multivibrator Q25 and Q26. It is the job of the Measure Store circuit to determine whether the A-D Converter will sample (Measurement Mode) the input voltage or continue to display the information held in storage (Storage Mode).

POLARITY SENSING

Q13 turns on only when a 1 period time pulse appears at its gate and in Measurement Mode. This activates the Polarity Sensing Circuit. If the voltage at R40 is positive (Negative instrument input) Q15 will conduct and the signal from the Measure Store Multivibrator (Q25) will cause FET switch Q16 to conduct placing input on the A-D Amplifier.

If the voltage sensed by R40 is negative (Positive input to the 8100) Q14 will conduct and the signal at the collector of Q14 and the pulse from the Measure Store Multivibrator Q25 will turn FET switches Q12 and Q17 on. The negative output of the Buffer will be applied through the scaling resistors R50 and R51 and switch Q12 to the negative input of the A-D Amplifier. The Polarity Detector operates only while the instrument is in the Measurement Mode of operation and serves no function in the Storage Mode.

During time period 1, the amplified remainder is applied to C35 Q35 is prevented from conducting during the first half of the time period by the clock signal which is coupled through CR36 to its gate. During the second half of the period Q35 is on and the amplified remainder is applied to C34.

During the second time period, Q35 is off and Q36 is on which applies the remainder stored in C34 to be applied to the input of the Amplifier. Q39 is switched on and the remainder is now applied to C35, during the second half of the time period. Q39 is switched off during the third time period and Q37 and Q38 are switched on which applied the remainder stored in C35 to be applied to the amplifier input.

During the third time period, second half, the remainder is stored in C34.

During the fourth and last time period Q34 is switched on and the final remainder stored in C34 is applied to the input of the Amplifier.

ANALOG STORAGE

Clock pulses being applied through CR19 to Q28 allow conduction only during the second half of each time period. Q30 through Q33 are enabled only during the time period pulse corresponding to its gate connection.

During the last half of the 1 period the output of the Secondary Ladder is stored in capacitor C30. During the last half of the second period, the output of the Secondary Ladder is stored in C31. Etc.....

Q29 is enabled only when the instrument is in the Storage Mode and applied the output of each of the storage capacitors to appear at the input to the amplifier.

Analog storage is used only when the instrument is in the Storage Mode of operation as determined by the Measure Store Multivibrator.

MEASURE STORE MULTIVIBRATOR

The one shot multivibrator formed by Q25 and Q26 has dual synchronizing inputs. The Measurement Cycle (approx. 20 ms) is coincident with the conduction of Q25. The Storage Cycle (approx. 330 ms) is coincident with the conduction of Q26. The multivibrator is triggered at the end of each complete cycle by the negative edge of the 4th time period pulse. If C29 is sufficiently discharged, this negative pulse will cause the multivibrator to pulse, sending a 20 ms measure pulse to the Polarity Sensing circuit which starts a measurement cycle. If the multivibrator does not pulse the 8100 remains in Storage Mode.

DISPLAY

It should be noted that each readout tube is on only during the last half of its corresponding time period. (2 ms on and 18 ms off)

The BCD output of the A4 Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 3 the Decoder Driver will apply ground to the three line to all readout tubes. The 1 time period pulse will enable Q67 and Q71 which will allow the +200 volt pulse, which occurs only during the second half of each time period to light the three digit in V1.

EXAMPLE OPERATION (Figure 4) (Example voltage is .6532v)

Counter A4 is reset to zero as it is at the beginning of every time period by the pulse from A3A NAND gate.

The Ring Counter produces the ZERO pulse and Q18 and Q58 are turned on. Q58 connects C37, the zero holding capacitor, to the output of amplifier A2. Q18 connects the positive input of the amplifier to ground. This operation removes the offset for the remainder of the measurement cycle.

The Ring Counter produces the 1 time period pulse. It is necessary to assume that Q25 in the Measure Store Multivibrator is conducting. The 1 pulse will turn transistor Q13 on. Since the .6532 volts into the instrument is positive, the voltage across R40 will be negative. Q14 will conduct which will cause Q12 and Q17 to turn on. These transistors were enabled by the Measure pulse from the Measure Store Multivibrator. The negative voltage from the Buffer will be applied to the A-D Amplifier through scaling resistors R50 and R51. Q17 connects the positive input to the amplifier to ground via resistors R186 and R187 which provide offset correction voltage to the positive input.

With R98 200 kΩ in the feedback loop and R51 and R50 as the input resistance the gain of the amplifier is 70. Q52 is used as temperature compensation only.

With .6532 volts at the input terminal of the amplifier, the output will attempt to go to 40 volts to satisfy the loop gain, but will be prevented from going so high by the limiting action of Q76 and R110. The output will exceed 7.0 volts and cause Q61 to conduct, supplying current to the Voltage Controlled Oscillator.

The Voltage Controlled Oscillator, Q59 and Q60, will supply a series of pulses when supplied current. The repitition rate will be proportional to the current being supplied.

The pulses from the VCO are applied to the Counter A4, which is reset at the start of each time period. This counter translates the pulses into Binary Coded Decimal output. This BCD output is applied to the Ladder Switches and Drivers. As the BCD numerical value increases, the ladders produce 0.1 volt steps in their output. Thus in this case when the Primary Ladder output reaches .6 volts and is fed back to the input of the A-D Amplifier, the input difference to the amplifier becomes .0532 volts and the output of the amplifier will be less than 7 volts. When this occurs the Analog Comparitor Q61 does not furnish current to the VCO which causes it to stop pulsing.

The Decoder Driver translates this BCD output to decimal and produces a ground potential that is fed to all of the readout tubes 6 line. The +200 volts pulses only during the last half of the time period, so during the last half of the time period the readout tube is lighted. Only the 1 tube will light since it is the only one enabled by the 1 pulse via Q67 and Q71.

The Secondary Ladder feeds the Analog Storage circuit. Q28 is enabled only during the second half of each time period and Q30 is enabled by the 1 time period pulse. This causes C30 to be charged to .6 volts being furnished by the Secondary Ladder.

The remainder voltage during time period 1 was 0.532 volts at the input to the A-D Amplifier. This remainder is multiplied by the amplifier to 3.724 volts and appears across remainder resistors R99, R100 and R149. It is apparent that the total resistance is 14 kΩ and that 2 kΩ represents 1/7 of the total resistance. This means that one seventh of the voltage appearing across the total remainder resistance appears across R100. This means, in the example case, .532 volts. This voltage will be applied across C34 in the Sample and Hold Circuit by the 1 time period pulse enabling transistor Q35. CR36 allows Q35 to be enabled only during the second half of the time period.

SUMMARY:

The highlights of the action that has taken place during the first time period are as follows:

1. The .6 volts was digitized.
2. .6 volts was placed in Analog Storage.
3. The remainder voltage .532 was placed in storage.
4. The 6 was displayed during the last half of the time period by V1.

Time period 1 ends and transistor Q13 is no longer enabled as the 1 pulse is no longer furnished to it.

At the start of time period pulse 2 enables Q36 which applied the .532 volt remainder stored in C34 to appear at the input to the A-D Amplifier via Q18 which is enabled for the entire duration of The Measure Cycle. The .532 volts is amplified by 70 and once again the output of the amplifier exceeds the 7 volt reference causing Q61 to furnsih current to the Voltage Controlled Oscillator. The pulse train produced is translated to BCD output and the Ladders are switched up in 0.1 volt increments until .5 volts is fed from the Primary Ladder to the summing junction of the A-D Amplifier. The input to the amplifier at this time is 0.32 volts which results in an output from the amplifier that is less than 7 volts and Q61 cuts off. The BCD output from the A4 Counter is applied to the Decoder Driver and translated to decimal output, placing ground potential on all of the "5" lines to the readout tubes. The 2 pulses enables Q68 and Q72 during

the entire time period but the +200 volt pulse only occurs during the last half of the time period. Thus the readout tube V2 will display the "5" only during that last half of the time period.

The Secondary ladder will have an output of .5 volts at this time and it will be stored on capacitor C31 during the last half of the time period when Q28 conducts and Q31 is enabled by the 2 pulse.

The remainder, .032 volts will be amplified and divided by the remainder resistors and will be stored in the Sample and Hold circuit capacitor C35 via the enabled Q39 as .32 volts.

During period "3" Q38 will be enabled and apply the .32 volts stored there across the input to the A-D Amplifier through Q27.

The amplified voltage from the output of the amplifier will exceed the 7 volts of reference and Q61 will supply current to the Voltage Controlled Oscillator which will start a pulse chain. The pulses will be translated into BCD output. The BCD output will switch both Ladders and be decimalized by the Decoder Driver. When the output of the Primary Ladder reaches .3 volts the output of the amplifier will be less than 7 volts and Q61 will stop supplying current to the VCO. The decimalized "3" will appear as a ground potential on all of the 3 lines to the readout tubes. During the last half of the time period the +200 will pulse on and Q69 and Q73 being enabled by the 3 pulse will allow V3 to display the digit 3.

The .3 volts from the Secondary Ladder will be stored in Analog Storage capacitor C32 during the lasthhalf of the time period when Q28 is enabled and the 3 pulse has enabled Q32.

The remainder .02 at the input of the amplifier is amplified and appears across the remainder resistors and will be divided down to .2 volts and Q37 will be enabled causing this remainder to be stored in C34.

During time period 4 Q34 conducts applying the .2 volts stored in C34 to appear on the input to the A-D Amplifier. The output will exceed the reference voltage causing Q61 to supply current to the VCO which will start a pulse train. Counter A4 will count the pulses and translate them to BCD output. This BCD output causes the Ladder switches to operate and the output from the Primary Ladder is fed back to the summing point of the A-D Amplifier. When the output reaches .2 volts, the output of the amplifier is no longer higher than 7 volts and Q61 will stop conducting. The VCO stops pulsing and the Decoder Driver will translate the BCD output to decimal and apply ground potential to the 2 lines to all of the readout tubes. The 4 pulse will enable Q70 and Q74, which will allow the +200 volts to light the tube V4 when it pulses on during the second half of the time period. The Secondary Ladder will have an output of .2 volts which will be stored in Analog Storage capacitor C33, the 4 pulse having enabled Q33 and the second half time period pulse having enabled Q28.

This completes a Measurement Cycle. As the 4 time pulse goes negative returning to zero potential it will cause Q25 (Measure Pulse) to conduct, only if capacitor C29 is sufficiently discharged. In this case it would not be possible for the instrument to start another Measurement Cycle as C29 would be fully charged.

SUMMARY:

It will be noted that each increment of voltage has been stored in the Analog Storage capacitors as follows:

C30 .6 volts

C31 .5 volts
C32 .3 volts
C33 .2 volts

None of these stored voltages were used in the Measurement Cycle. C29 was fully charged and Q26 is conducting, which occurs during the Storage Cycles of the instrument. Q27 will be off and Q29 will be enabled until the Measure Store Multivibrator is operated again. Q26 will conduct for approximately 330 ms or about 16 cycles of the instrument. At that time C29 will be sufficiently discharged to allow Q25 to conduct when it receives a negative going pulse from the 4th time period pulse. Q25 will then conduct for approximately 20 ms or one Measurement cycle.

STORAGE CYCLE

The ZERO pulse will again cause the offset to be removed from the A-D Amplifier by placing C37 across the output of the amplifier and grounding the input, as the result of Q18 and Q58 conducting.

The 1 pulse will cause Q30 to enable and the voltage stored on C30 (0.6 volts) to be applied to the input of the A-D Amplifier through Q29, which has been enabled by the Measure Store Multivibrator.

The A-D Amplifier amplifies the .6 volts by 70 and the output of the A-D Amplifier exceeds the 7 volt reference causing C61 to conduct and supply current to the VCO. The VCO will start producing a pulse train. These pulses are counted and translated into BCD output by the action of Counter A4. The BCD output causes the Ladders to switch and increase their output by .1 volt per pulse. When the output of the Primary Ladder reaches .6 volts it will cause the A-D Amplifier to be satisfied and it will no longer have an output that is above the 7 volt reference of the instrument. The Secondary Ladder will have produced a .6 volt output which will be stored in C30 during the second half of the time period via Q28.

The Decoder Driver will have translated the BCD output to decimal and applied ground to all of the readout lamps on the 6 line. Q67 and Q71 are enabled by the 1 pulse and when the +200 volts pulses on, as it does during the second half of the time period V1 will display the 6.

During time period 2 Q31 and Q29 conducting will cause the .5 volts stored in C31 to appear across the input to the A-D Amplifier. The amplifier will have an output of more than 7 volts, which will cause Q61 to conduct and supply current to the VCO, which will produce a pulse train. The Counter A4 will count and translate the output to BCD. The Ladders will produce .1 volt of output for every pulse. The Primary Ladder being fed back to the input of the A-D Amplifier will cause the output of that amplifier to drop below 7 volts when .5 volts level is reached, which will cause Q61 to cut off and the VCO to stop producing pulses.

The Secondary Ladder will have produced .5 volts which will be stored on C31 during the second half of the time period by the conduction of Q28. The Decoder Driver will have placed ground potential on the 5 lines to the readout tubes. Q68 and Q72 will be enabled by the 1 pulse and during the second half of the time period the +200 volts will pulse on cuasing V2 to display the digit 5.

During the 3 time period, Q32 will be enabled placing the .3 volts stored in C32 to be applied to the A-D Amplifier. The output of the amplifier will exceed the 7 volt reference and Q61 will supply current to the VCO which produces a pulse train. The pulses will be counted and trans-

lated to BCD output. This BCD output will cause the ladder switches to operate and increase the output of both ladders to increase by .1 volt for every pulse of the VCO. When the output of the Primary Ladder reaches .3 volts the A-D Amplifier will be satisfied and its output will drop below 7 volts causing Q61 to stop conducting, and the VCO will stop pulsing. The output of the Secondary Ladder (.3 volts) will be stored on C32 during the second half of the time period through Q28 which conducts only during the second half of each time period.

The Decoder Driver will have translated the BCD output to decimal and placed ground potential on all of the 3 lines to the readout tubes. Q69 and Q73 will have been enabled by the 3 time pulse and the 3 will be displayed by V3 when the +200 volts pulses during the second half of the time period.

Time pulse 4 will cause the .2 volts on C33 to be placed on the input to the A-D Amplifier whose output will exceed the 7 volt reference. Q61 will conduct and the VCO will pulse causing the ladder outputs to step .1 volt for every pulse received. When the output of the Primary Ladder, which is fed back to the summing point, reaches .2 volts, the output of the amplifier will no longer be higher than the 7 volt reference and Q61 will stop supplying current to the VCO. The Secondary Ladder will charge C33 to .2 volts and the action of the Decoder Driver will cause ground potential to appear on all of the 2 lines to the readout tubes. Q70 and Q74 will be enabled and when the +200 volts pulses during the second half of the time period, V4 will display the 2.

SUMMARY:

The capacitors in the Analog Storage Circuit will contain all of the increments of the voltage that were digitized during the previous Measurement Cycle. The Sample and Hold Circuit is disabled during all Storage Cycles. Each digit is displayed only during the last half of each time period. During the Storage Cycle the Polarity Sensing Circuit is not enabled.

This completes the Storage Cycle and as previously explained, the instrument will enter another Storage Cycle unless the charge on capacitor C29 has decreased to a value low enough to cause the Measure Store Multivibrator to pulse. If the Multivibrator does pulse a new Measurement Cycle will start and the input will be sampled again.

TROUBLESHOOTING:

1. There are several ways of isolating the section of the 8100 that is malfunctioning. Observation of the readout and logical deduction baised upon the knowledge of the theory of operation may be adequate to sectionalize the trouble.

2. The Power Supplies are interrelated and to isolate troubles in this area it may be necessary to isolate the −18 volt supply. To do this, disconnect the +15 volt end of R5 and connect it to an external source, or disconnect R34 and place a 1330Ω ±1% resistor from the base of Q3 to ground.

3. The Input Buffer can be checked by measuring the voltage between TP9 and TP1 (ground), while measuring a voltage in the 1 volt DC range. The voltage measured should be the same as the input but in reverse polarity.

4. The Auto Zero circuit will mask many types of trouble, so to disable this circuit it will be necessary to jumper TP6 to TP7 and jumper −18 volts to TP8. The measurement will now have an offset but the Auto Zero will be disabled.

5. Storage Mode can be avoided and the instrument placed in continuous Measurement Mode by placing a jumper between TP4 and TP5.

6. Connect +15 volt supply to the junction of R60 and R61, the Ring Counter will stop and the instrument will no longer display anything in the readout tubes. All of the output lines should measure −18 volts at this time. Remove the jumper and measure the collector voltage with an oscilloscope, each collector should measure about .3 volts when the transistor conducts.

7. An excessive load on any Ring Counter output can cause it to oscillate. Spikes following the time pulse indicate that the Ring Counter is near oscillation.

8. Trailing edge droop on the time pulses is caused by low gain transistors Q20 through Q28.

9. The following procedure will check the operation of the A-D Amplifier;

   a. Disable the Ring Counter by placing a jumper from +15 volts to TP11.

   b. Disable the Measure Store Multivibrator by placing a jumper from TP4 to TP5.

   c. Enable the Polarity Sense by placing a jumper from Q31 source to Q31 drain.

   d. Remove Binary Counter A4.

   e. Measure the voltage between TP2 and TP1 (ground).

   f. Apply 100 mv increments of input to the 8100. The measured voltage should increase 350 mv for every 100 mv increment of input and will be of the same polarity.

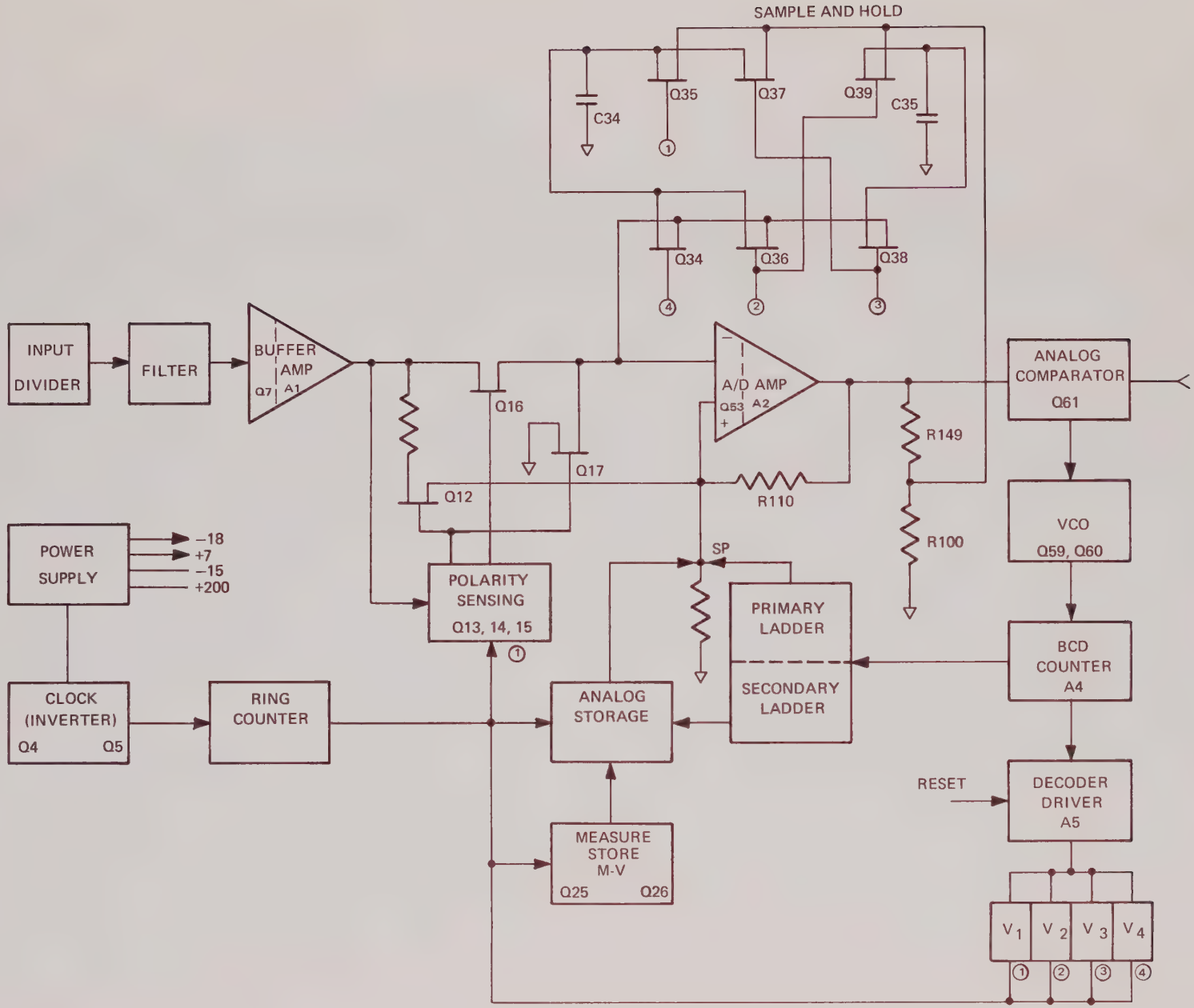


Figure 1. 8100 BLOCK DIAGRAM

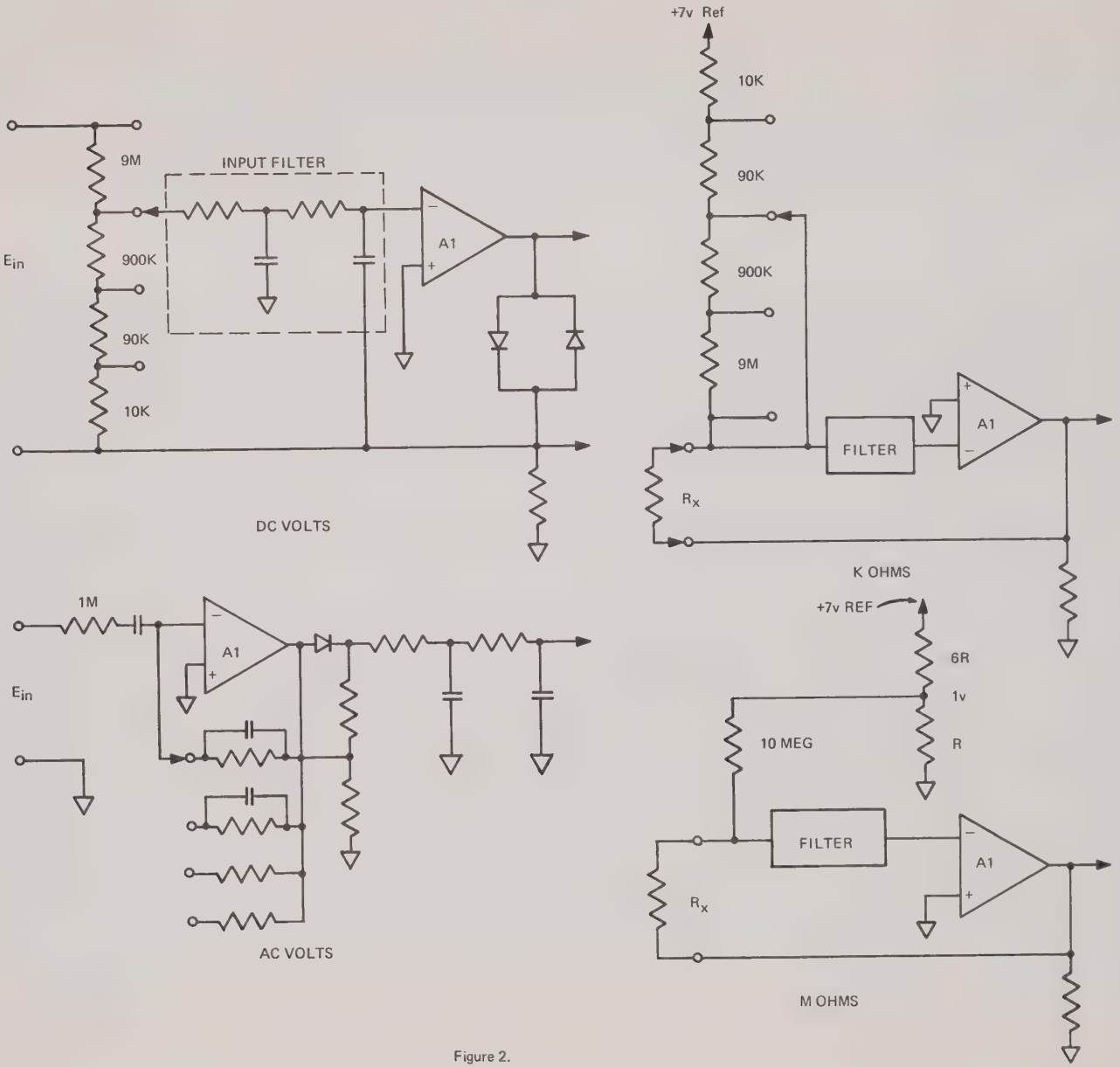

9M
INPUT FILTER
E_{in}
900K
90K
10K
A1
DC VOLTS
1M
E_{in}
A1
AC VOLTS
+7v Ref
10K
90K
900K
9M
FILTER
A1
R_x
K OHMS
+7v REF
6R
1v
R
10 MEG
FILTER
A1
R_x
M OHMS

Figure 2.

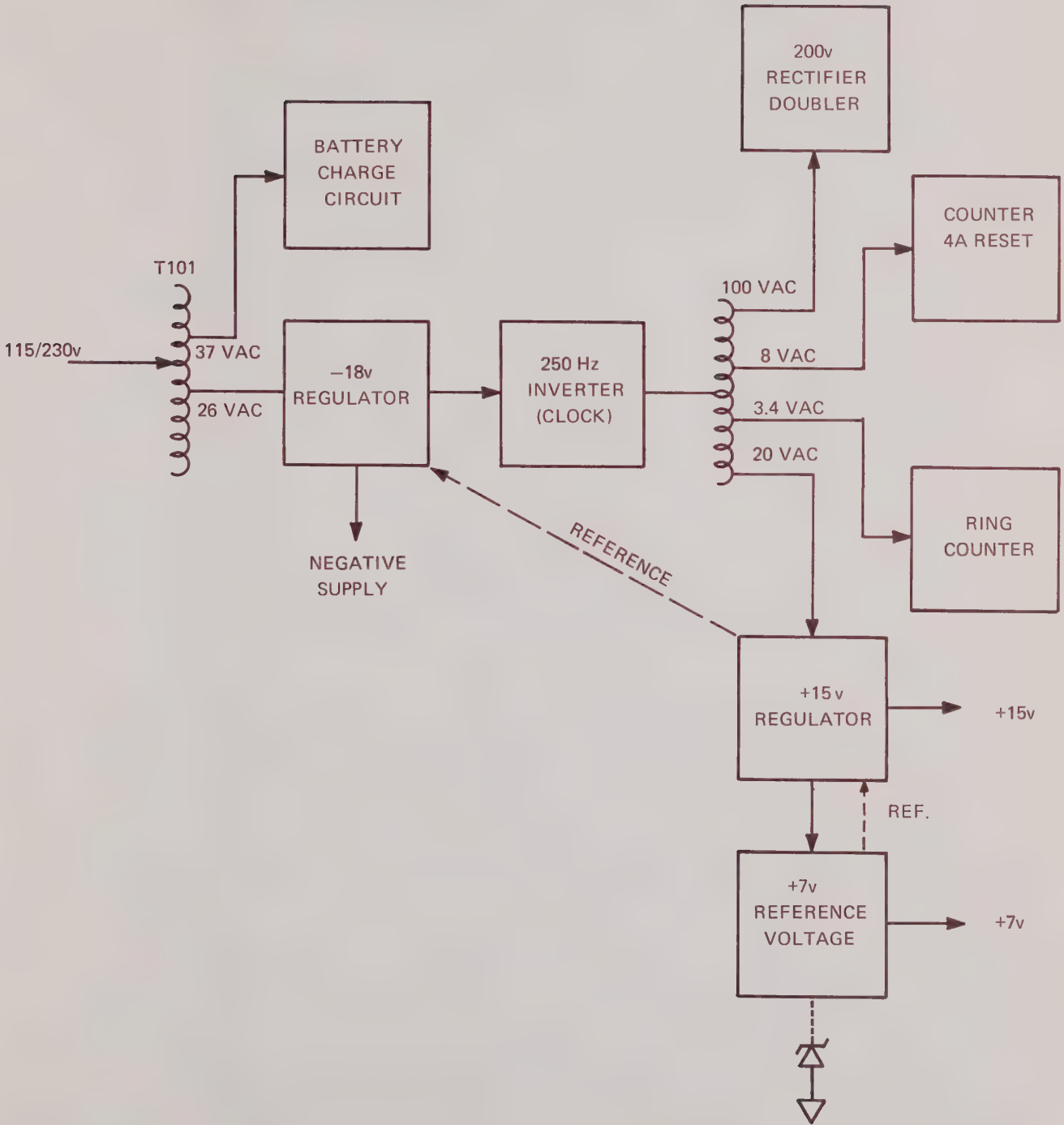


Figure 3. 8100 POWER SUPPLY

MEASURE MODE	ZERO	1	2	3	4
Q18 & Q58 conduct and remove offset from A-D amp.					
1 from Ring Counter enables Q13, polarity is determined and input FETs apply .6532 to A-D. 6 is digitized, remainder is stored in S & H C34. 6 is displayed and .6v stored in C30.					
Input is disconnected from A-D amplifier.					
.532v from C34 is applied to A-D input. 5 is digitized and remainder .32 is stored in S & H C35. 5 is displayed and .5v is stored in C31.					
.32 from C35 is applied to A-D amplifier. 3 is digitized and remainder .2 is stored in C34. 3 is displayed and .3v is stored in C32.					
.2v from C34 is applied to A-D input and digitized. 2 is displayed and .2v is stored in C33.					
STORAGE MODE	**ZERO**	**1**	**2**	**3**	**4**
Q18 & Q58 conduct and remove offset from A-D amp.					
Q30 conducts and applies .6v from C30 to A-D amp. 6 is digitized 6 is displayed and .6v is restored to C30.					
Q31 conducts and applies .5v from C31 to A-D amp. 5 is digitized 5 is displayed and .5v is restored to C31.					
Q32 conducts and applies .3v from C32 to A-D amp. 3 is digitized. 3 is displayed and .3v is restored to C32.					
Q33 conducts and applies .2v from C33 to A-D amp. 2 is digitized. 2 is displayed and .2v is restored to C33.					

NOTE: If C29 is sufficiently discharged, the negative going portion of the 4 pulse will trigger the Measure Store Multivibrator and a measure pulse will be generated and a measure cycle will be started. If not another storage cycle will start.

Figure 4.

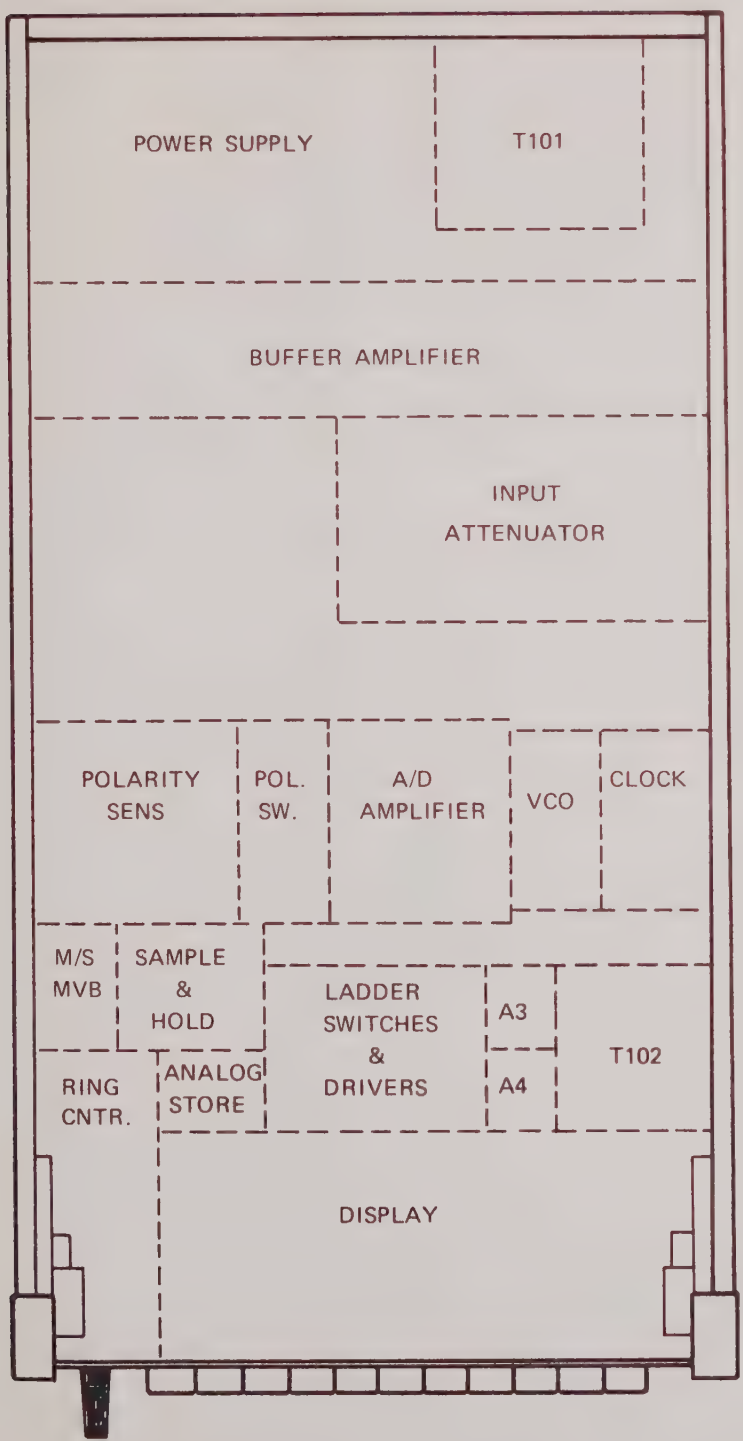
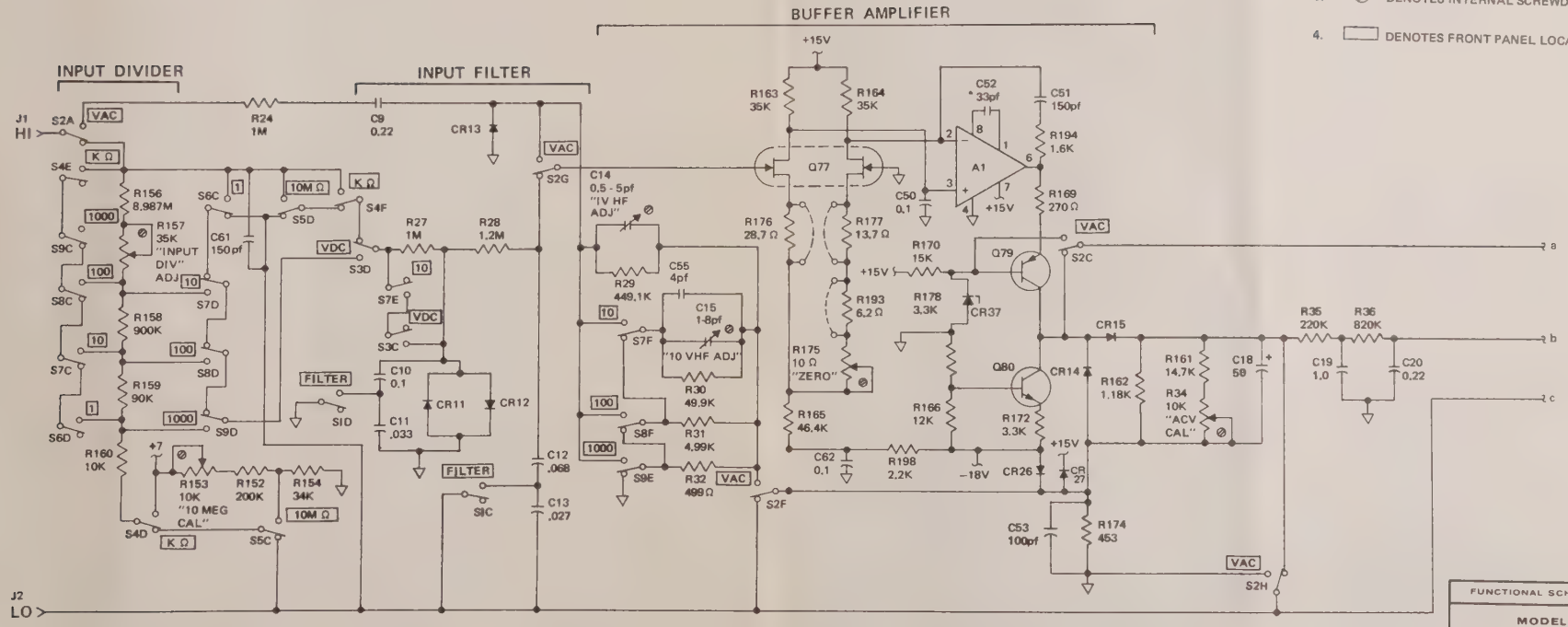


Figure 5. 8100 LAYOUT

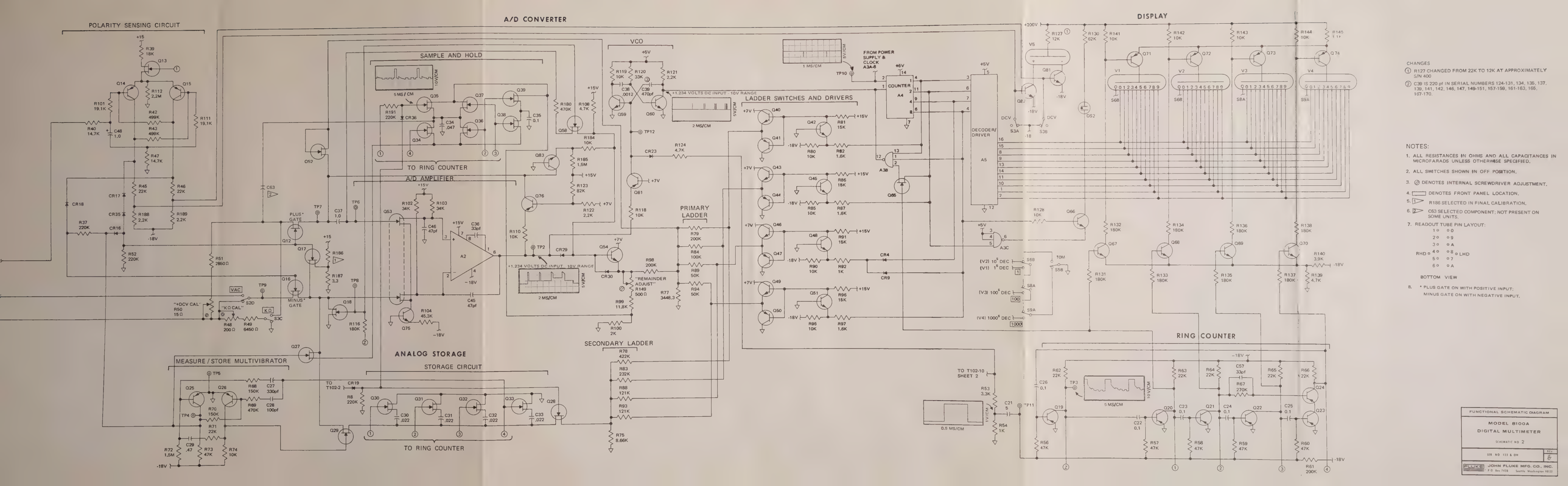
BUFFER

NOTES;

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.



FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER	
SCHEMATIC NO 1	
SER NO 123 & ON	REV 6
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



CHANGES

(1) R127 CHANGED FROM 22K TO 12K AT APPROXIMATELY S/N 400

(2) C39 IS 220 pf IN SERIAL NUMBERS 124-131, 134, 136, 137, 139, 141, 142, 146, 147, 149-151, 157-159, 161-163, 165, 167-170.

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. ▷ R186 SELECTED IN FINAL CALIBRATION.
6. ▱ C63 SELECTED COMPONENT; NOT PRESENT ON SOME UNITS.
7. READOUT TUBE PIN LAYOUT:

RHD: 1 o 0, 2 o 9, 3 o A, 4 o 8, 5 o 7, 6 o A; o LHD

BOTTOM VIEW

8. * PLUS GATE ON WITH POSITIVE INPUT; MINUS GATE ON WITH NEGATIVE INPUT.

FUNCTIONAL SCHEMATIC DIAGRAM

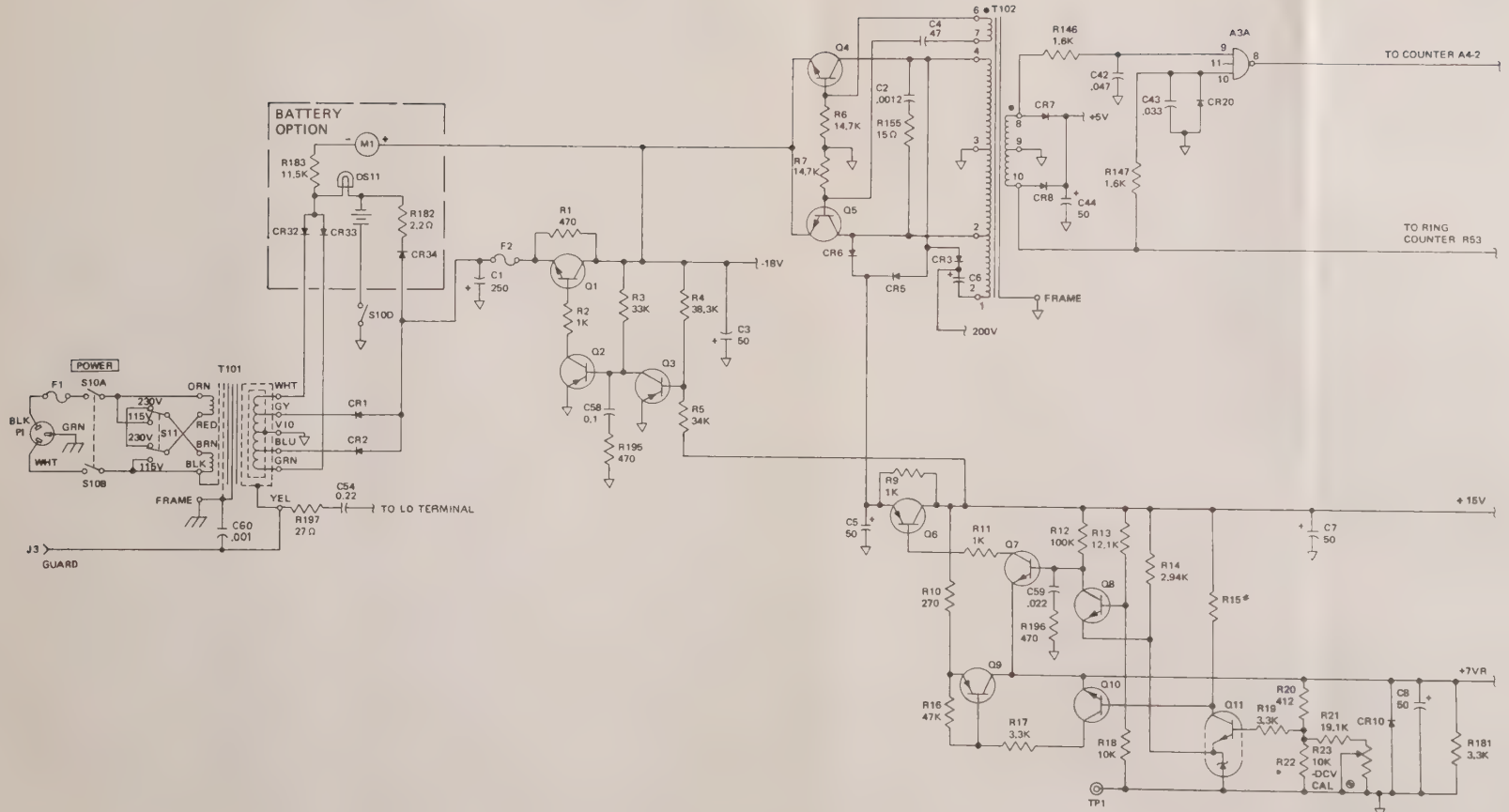
MODEL 8100A
DIGITAL MULTIMETER

SCHEMATIC NO. 2

SER. NO. 133 & ON

REV. A

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



1 *RESISTOR VALUE SELECTED AT TEST OF Q11

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8100A
DIGITAL MULTIMETER

SCHEMATIC NO 8

SER NO 123 & ON

REV 6

FLUKE JOHN FLUKE MFG. CO., INC
P.O. Box 7428 Seattle, Washington 98133

TECHNICAL DATA FILE

JOHN FLUKE MFG. CO., INC. ■ MODEL **8300A**

FLUKE

DIGITAL VOLTMETER

FEATURES

BASIC:

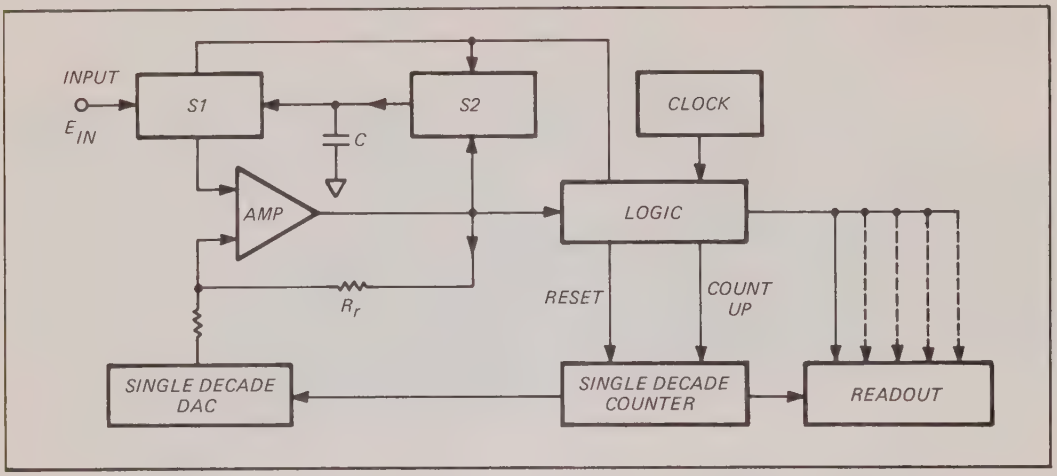
- *3 RANGES DC TO ±1100V — AUTO RANGE AND AUTO POLARITY*
- *"RECIRCULATING REMAINDER"* A/D CONVERSION FOR HIGH RELIABILITY*
- *FULL 5 DIGITS + "1" FOR 20% OVERRANGING*
- *ACTIVE 3-POLE SWITCHABLE FILTER WITH 60 Hz NOTCH*
- *40 READINGS PER SECOND FOR SYSTEMS APPLICATIONS*

OPTIONS:

- *AC VOLTAGE MEASUREMENTS IN 4 RANGES FROM 0 TO 1100 VOLTS*
- *MILLIVOLT/FOUR TERMINAL OHMS IN ONE OPTION*
- *ISOLATED EXTERNAL REFERENCE ALLOWING 4-WIRE BIPOLAR RATIO MEASUREMENT*
- *ISOLATED DIGITAL DATA OUTPUT IN SERIAL OR PARALLEL FORMAT*
- *ISOLATED REMOTE CONTROL*

* Patent Pending

The 8300A is a versatile digital voltmeter with five full decades of digits plus a 6th digit for 20% overrange. Its mainframe will accept all options at any time, in any sequence for expansion from a bench DVM into a bench or systems multimeter.



Fluke's new and unique "Recirculating Remainder" A/D conversion technique is used in the 8300A. Its conversion circuitry periodically samples the input and serially digitizes the sample.

At the beginning of a conversion cycle, switch S1 connects E_{in} to the AMPlifiers input. The amplifier acts first as a comparator with its output stimulating the LOGIC to instruct the SINGLE DECADE COUNTER to count up the SINGLE DECADE DAC until its output equals the most significant digit (MSD) of the input. The remainder (difference) voltage of E_{in} − MSD is multiplied by 10 because remainder resistor R_r provides feedback for precise control of amplifier gain following determination of the MSD. The amplified remainder, 10 (E_{in} − MSD), is stored on capacitor C via switch S2 and the registered count is transferred to the READOUTs first digit.

Following display, the counter is reset to zero and S2 opened. S1 disconnects from E_{in} and connects the voltage on C to the amplifier. Second digit conversion is accomplished with the same circuits and procedures used to determine the first digit. The registered count is transferred to the readouts second digit and a new remainder stored on C.

Conversion is repeated three more times in the FLUKE 8300A using remainder voltages stored from the immediately preceeding conversion.

"Recirculating Remainder" conversion circuitry is characterized by a low total parts count and extremely low power consumption.

Autoranging is a standard feature of the 8300A although preselected ranges may be programmed manually via front panel pushbutton switches or with the remote control option. Functions are also manually programmed at the front panel or remotely by option. The pushbutton switches are interlocked to prevent simultaneous operation of incompatible functions or ranges. All switches are installed in the basic 8300A whether the function is or not.

The left side of the readout illuminates to display the function called, polarity for DCV and MV, presence of filter and an overload warning. The readout does not illuminate for optional functions that are not installed. The readouts neon tubes are non-blinking and decimal point positioning is automatic.

Measurement of noisy inputs is enhanced by manual or remote (optional) programming of the 8300A's active 3-pole filter. The filter has a notch at 60 Hz and is buffered to eliminate "kick-back" and input impedance changes.

The 8300A's sample rate can be manually varied from the front panel or it can be remotely controlled (optional).

Full guarding is accomplished by box-in-a-box construction and use of a FLUKE custom-designed isolating power transformer. Guarding is not compromised when the isolated Data Output and Remote Control units are added.

Calibration is accomplished through the guard via labelled ports.

ANALOG OPTIONS

All options may be installed in the field or factory for the same price. The analog options are fully within the guard, their installation automatically enables the appropriate function light of the display. Options are calibrated and ready for immediate use when field installed.

AC volts features a 50 Hz to 20 KHz midband with good accuracy to 30 Hz and 100 KHz. The AC converters output is the average rectified value of the AC input scaled to digitize as the RMS value of a sine wave.

Mv/Ohms extends the DC capability of the 8300A to 100 mv at full range with 1 uv of resolution. It includes 5 resistance ranges, using a modified four-terminal configuration on the two lowest.

External Reference can be used for true four-terminal ratio or for systems measurements related to a master reference.

DIGITAL OPTIONS

Data Output is completely isolated from the analog input and is available in a 8–4–2–1 BCD logic level format. Data is transferred serially via guarded toroids from the 8300A to the Data Output unit. Single decade code conversion and serial-character, parallel-bit acquisitions are unique capabilities in addition to standard full parallel output.

Remote Control is fully isolated from analog input and may be fully isolated from the Data Output unit but is normally used in conjunction with it. Control is exerted by logic levels or contact closures. Isolation from analog circuitry is accomplished through the use of light-emitting diodes and photo-transistors.

SPECIFICATIONS

DC VOLTS

RANGES . . . . . ±10V, ±100V and ±1000V. 20% overrange capability (1100V maximum)

POLARITY: . . . . . Automatic, instantaneous selection and display.

RANGE SELECTION: . . . . . Manual and autorange standard (Remote optional)

RESOLUTION: . . . . . 0.001% of range (100 uv on 10V range)

ACCURACY:

24 hours, 23°C ±1°C . . . . . ±(0.005% of input + 0.001% of range)
30 days, 20°C to 30°C . . . . . ±(0.01% of input + 0.002% of range)
90 days, 20°C to 30°C . . . . . ±(0.01% of input + 0.003% of range)

TEMPERATURE COEFFICIENT

0°C to 20°C, 30°C to 50°C. . . . . ±(0.0007% of input + 0.0003% of range)/° C

INPUT RESISTANCE:

10V RANGE . . . . . 10,000 megohms minimum.
100V & 1000V RANGES . . . . . 10 Megohms.

FILTER . . . . . Switch selected 3 pole active filter standard (remote control optional)

RESPONSE TIME:

INCLUDING POLARITY CHANGE . . . . . To within 0.01% of step function change.
25 ms maximum unfiltered. (No settling time required for input applied coincident with read command. Time given is digitizing time only.)
500 ms maximum filtered.
NOTE: Filter settling time unaffected by source impedance.

REJECTION:

	DC	AC
Normal Mode (Filtered)	–	>60 db, above 50 Hz
Common Mode (Unfiltered) 1 KΩ unbalance in either lead 100Ω unbalance in either lead	 >140 db >160 db	 >100 db, 60 Hz and above. >120 db, 60 Hz and above.
Common Mode (Filtered) 1 KΩ unbalance in either lead	>140 db	>140 db, 60 Hz and above.

MAXIMUM NORMAL MODE VOLTAGE . . . . . 50% of range, peak AC.

MAXIMUM COMMON MODE VOLTAGE . . . . . 1000V DC or peak AC.

ADDITIONAL SPECIFICATIONS BASIC DC UNIT 1100V DC or RMS (1500V peak AC) overload with no damage (any range).
Input capacitance < 100 pf.
Input offset current less than 50 pa on any range.

DC MILLIVOLTS (USING MV/OHMS OPTION 8300A-02)

RANGES . . . . . ±100 mv and ±1000 mv. 20% overrange capability
(Up to 1100V overload with no damage)

POLARITY . . . . . Automatic, instantaneous selection and display.

RANGE SELECTION . . . . . Manual and autorange standard (Remote optional)

RESOLUTION . . . . . 0.001% of range
(1 uv on 100 mv range)

ACCURACY

90 days, 20°C to 30°C . . . . . 1000 mv range ±(0.01% of input + 0.003% of range)*

100 mv range ±(0.01% of input + 0.01% of range)*

*ZERO STABILITY (after 30 minute warmup) Better than 8 uv for 90 days. (Front panel millivolt zero control provided to compensate for external thermal EMFs, etc.)

TEMPERATURE COEFFICIENT:

0°C to 20°C, 30°C to 50°C. . . . . 1000 mv range ±(0.0007% of input + 0.0003% of range)/°C

100 mv range ±(0.0007% of input + 0.0005% of range)/°C

INPUT RESISTANCE:

1000 mv Range . . . . . 1000 megohms minimum.
100 mv Range . . . . . 100 megohms minimum.

RESPONSE TIME: (Including polarity change, to within 0.01% of step function change)

1000 mv Range . . . . . 1 second maximum.

100 mv Range . . . . . 3 seconds maximum.

NOTE: Response time figures applicable for source resistance up to 50 KΩ

REJECTION:

	DC	INTERFERENCE FREQUENCY	
		50 Hz	60 Hz
Normal Mode	–	> 55 db	> 60 db, 60 Hz and above
Common Mode 1 KΩ unbalance in either lead	> 140 db, DC to 60 Hz		

MAXIMUM INPUT VOLTAGE . . . . . 1100 VDC or RMS (1500V peak AC) overload with no damage (any range)

AC VOLTS (USING AC OPTION 8300A-01)

RANGES . . . . . 1V, 10V, 100V and 1000V
20% overrange capability (1100V RMS maximum)

RANGE SELECTION . . . . . Manual and autorange standard (Remote Optional)

RESOLUTION . . . . . 0.001% of range (10 uv on 1V range)

ACCURACY:
20°C to 30°C

	INPUT VOLTAGE	
FREQUENCY RANGE	.001V – 500V	500 – 1000V
50 Hz – 20 KHz	±(0.1% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	±0.15% of input
20 KHz – 50 KHz	±(0.2% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	±0.2% of input **
30 – 50 Hz and 50 KHz – 100 KHz	±(0.5% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	**

* Using front panel AC zero control periodically (typically 8 to 24 hours after 30 minute warmup) 30 and 90 day specifications apply if front panel zero is not used.

** Input Volt–Hertz product should not exceed 2×10^7.

TEMPERATURE COEFFICIENT

0°C to 20°C, 30°C to 50°C . . . . . ±(0.002% of input + 0.001% of range)/°C.

INPUT IMPEDANCE

(All Ranges) . . . . . 1 megohm shunted by < 100 pf

RESPONSE TIME:

(To within 0.1% of step function change) . . . . 500 ms maximum.

MAXIMUM INPUT VOLTAGE . . . . . 1100V RMS
(Up to ±1100V superimposed DC is allowed if the peak voltage does not exceed 1500V).

REJECTION:

Common Mode (DC to 60 Hz) . . . . . 100Ω unbalance in either lead. > 120 db

Maximum Common Mode Voltage . . . . . 1000V DC or peak AC.

OHMS (USING MV/OHMS OPTION 8300A-01)

RANGES . . . . . 1KΩ, 10KΩ, 100KΩ, 1000KΩ, 10MΩ. 20% overrange capability all ranges.

RANGE SELECTION . . . . . Manual and autorange 1 KΩ through 1000KΩ ranges.
10 MΩ range selected manually.
(Remote selection optional all ranges).

RESOLUTION . . . . . 0.001% of range
(10 milliohms on 1K range)

ACCURACY:

90 days, 20°C to 30°C . . . . . 1 KΩ, 10 KΩ, 100 KΩ Ranges
±(0.01% of input + 0.003% of range)

1000 KΩ Range
±(0.02% of input + 0.003% of range)

10 MΩ Range
±(0.05% of input + 0.003% of range)

TEMPERATURE COEFFICIENT:

0°C to 20°C, 30°C to 50°C . . . . . KΩ Ranges
±(0.0007% of input + 0.0003% of range)/°C

10 MΩ Range
±(0.003% of input + 0.003% of range)/°C

MEASUREMENT CURRENT:
(And Mode)

Range (KΩ)	1	10	100	1000	10 MΩ
Current (ua)	1.1 ma	110	100	10	1
Mode	4 terminal		2 terminal		

NOTE: Power dissipated in unknown resistor is only 1.2 milliwatts at 1 KΩ

RESPONSE TIME:
(To within 0.01% of step function change)

RANGE	UNFILTERED	FILTERED
1 KΩ 10 KΩ	1 sec	1.5 sec
100 KΩ, 1000 KΩ	25 ms *	
10 MΩ,	50 ms *	

* Includes 25 ms digitizing time-- No settling time required on 100 K & 1000K ranges for input applied coincident with read command.

MAXIMUM INPUT VOLTAGE . . . . . 30V RMS opens protective fuse.

4-WIRE RATIO (USING ISOLATED EXTERNAL REFERENCE OPTION 8300A-05)

RANGES:

MODE	RATIO RANGE ($\frac{A}{B}$)	READING	V INPUT (A)	V REF. (B)
DC/DC	0 ± 1.0	0 ±10.0000	0 ±10V	+2V to +10.5V Standard
	0 ± 10	0 ±100.000	0 ±100V	
	0 ± 100	0 ±1000.00	0 ±1000V	
MV/DC	0 ±0.01	0 ±100.000	0 ±100 mv	
	0 ±0.1	0 ±1000.00	0 ±1000 mv	

NOTE: DC External Reference may also be used for AC measurements.

20% overranging, autorange and autopolarity operation apply to V input for all modes above as applicable.

ACCURACY:

90 days, 20°C to 30°C . . . . . Same as basic DC except "% of range" must be modified to "% $\left(\frac{10V}{V\ REF}\right)$ of range".

Example: DC/DC ±(0.01% of reading + 0.003% $\left(\frac{10V}{V\ REF}\right)$ of range)

EXTERNAL REFERENCE INPUT SPECIFICATIONS:

Input Impedance . . . . . 1 megohm.

Response Time . . . . . To within 0.01% of step function change (2 seconds).

NORMAL MODE REJECTION: . . . . . > 30 db at 60 Hz.

ISOLATION: . . . . . Algebraic sum of V input + common difference voltage not to exceed 13V on 10V range and MV ranges.
(input & reference commons)

GENERAL:

DISPLAY	Function/polarity display block plus six digit in-line neon readout.
DIGITIZING TIME	25 ms maximum.
SAMPLE RATE	Front panel variable from 10 readings/sec to 1 reading/3 sec + "EXT" (External Control) position. 40 reading/sec under external control through the Data Output Unit.
MAXIMUM INPUTS:	
"HI" to "LO"	See individual function specifications.
"LO" to "GUARD"	100V
"GUARD" to "GROUND"	1000V DC or peak AC.
TEMPERATURE RANGE	Operating 0°C to 50°C Storage –40°C to +75°C
HUMIDITY RANGE	Operating < 70% relative humidity; 25°C to 50°C < 80% relative humidity; 0°C to 25°C
ALTITUDE	Operating 10,000 Feet. Non Operating 50,000 Feet.
SHOCK & VIBRATION	Meets requirements of MIL-T-21200G and MIL-E-16400F.
POWER	115/230V, ±10%, 50-440 Hz line, 20 watts with all options.
WARMUP TIME	30 minutes to meet all specifications.
WEIGHT	15 lbs basic. 19 lbs with all options.
SIZE	3.5" high by 17.5" wide by 15" deep (see outline drawing)

PRICE:

8300A	$1295
8300A-01 AC	$450
8300A-02 MV/Ohms	$350
8300A-03 Data Output Unit	$500
8300A-04 Remote Control Unit*	$200
8300A-05 External Reference (Ratio) (requires -07)	$200
8300A-06 Rear Input (requires -07)	$15
8300A-07 Rear Terminal Accessory**	$25

*Remote control unit requires Data Output Unit, 8300A-03. If Remote Control Unit only is needed, consult factory.

**-07 required with -05 or -06.

NOTE: When ordering an option for field installation, prefix the option number with "8300A" and suffix it with "K". e.g. 8300A-01K.

REMOTE CONTROL (Using REMOTE CONTROL option 8300A-04)

INPUTS		LINES	LOGIC LEVELS	
Function:	DCV, MV, ACV, KΩ, MΩ Filtered, External Reference	7	0 to +0.5V (or contact closure)	+5V (or open)
			Function Called	Function inactive
Range:	1, 10, 100, 1000 uncoded	4	Range Called	All lines open Autorange

Input is series 930 DTL

INTERLOCKS	Interlocks are provided to disallow multiple function or range calls for incompatible combinations.
POWER	+5V power available from Data Output Unit (May be externally powered – 5V DC at 150 ma required).
ISOLATION	All CMRR specifications apply with RCU installed. 1000 VDC or peak AC may be applied between RCU common and input "LO".

8300A SPECIFICATIONS

DATA OUTPUT UNIT: (USING DATA OUTPUT OPTION 8300A-03)

OUTPUTS	LINES	LOGIC LEVELS	
		0 to +0.5V	+5V
FUNCTION: DCV, MV, ACV, KΩ, MΩ Filter, External Reference	7	Function inactive.	Function called.
RANGE (Coded): 1 = 00, 10 = 01, 100 = 10, 1000 = 11	2	Logic 0	Logic 1
POLARITY:	1	Negative	Positive
6 DIGITS (Including "Overrange "1") Binary-Coded Decimal 8-4-2-1	21	Logic 0	Logic 1
DATA READY (Print) COMMAND	1	Data Ready	Data Blanked
OVERLOAD FLAG	1	No Overload	Overload
+5V REF & RETURN (TO POWER RCU)	2	----	----
INPUTS		0 to +0.5V	+5V (or open)
EXT. TRIGGER (Read Command)	1	+5V pulse > 1 usec	
SAMPLE TIME (Programmed Timeout)	1	Fast	Normal
INHIBITS (Address Lines For) (Serial Acquisition)	10	Inhibit	Normal

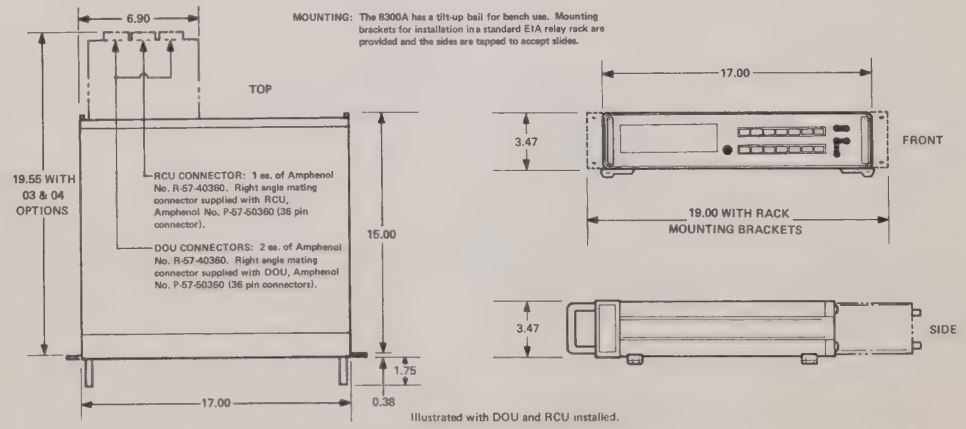
NOTE: 8 additional output lines and 4 input lines provided for code conversion of output data -- contact factory. Output is series 930 DTL with 6K collector resistors.

OUTPUT FORMAT . . . . . Complete parallel and addressable for parallel bit-serial character in multiples of 4 bits.

BLANKING . . . . . All outputs are high during conversion and programmed time outs — outputs enabled at time "Data Ready" flag appears.

POWER . . . . . +5V DC available as output to power remote control unit if desired.

ISOLATION . . . . . All CMRR specifications apply with DOU installed. 1000 VDC or peak AC may be applied between DOU common and input "LO".


6.90
MOUNTING: The 8300A has a tilt-up bail for bench use. Mounting brackets for installation in a standard EIA relay rack are provided and the sides are tapped to accept slides.
TOP
19.55 WITH 03 & 04 OPTIONS
RCU CONNECTOR: 1 ea. of Amphenol No. R-57-40360. Right angle mating connector supplied with RCU, Amphenol No. P-57-50360 (36 pin connector).
DOU CONNECTORS: 2 ea. of Amphenol No. R-57-40360. Right angle mating connector supplied with DOU, Amphenol No. P-57-50360 (36 pin connectors).
15.00
1.75
0.38
17.00
17.00
3.47
FRONT
19.00 WITH RACK MOUNTING BRACKETS
3.47
SIDE

Illustrated with DOU and RCU installed.

Litho In U.S.A.

FLUKE

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TWX 910-449-2850
Cable: FLUKE

II. BLOCK FUNCTIONS: (Figure 1)

A. Power Supply

The Power supply furnishes five voltages used in the insturment. +18, −18 operating supplies, +190 volt readout tube supply, +5 volt logic supply and +7 volt reference supply. Provisions are made for auxilary supply of 5 volts required in the Data Output Unit option.

B. Buffer

The Buffer board assembly includes Function switching components. It has an input impedance that is greater than 10^{12} with an insertion current less than 50 pa. The Input Attenuator offers three ratios of voltage division 1/1, 1/10 and 1/100. Input limiting is provided to prevent damage to the instrument in any range with up to 1100 volts applied.

The total gain of the Buffer is 1 inverted with a low impedance output. Input filtering is included in this assembly which consists of a 60 Hz notch filter and a 3 pole low pass (30 Hz) filter. All frequencies above 50 Hz are attenuated by more than 60 db.

C. Logic Section

A clock which operates at a frequency of 333 Hz produces a pulse train of 1.5 ms pulses, provides the timing for the entire instrument.

A 6 State Register divides the Clock pulses into six discrete time periods, which correspond to the ZERO time and the five digit times used in the instrument.

Current Controlled Oscillator provides a series of pulses that correspond to the digitalized value of the digit being converted from analog to digital value.

16 State Binary Counter receives the pulses from the Current Controlled Oscillator and converts them to Binary Coded Decimal (BCD) output in the standard 1-2-4-4 output.

Manual Range Controls are interlocked mechanically and electrically so as to provide priority to manual selections of function and range, preventing erronious dial function or range commands.

Auto Range Controls are provided to accomplish automatic selection of the proper range via reed relays and functional logic packs.

Sample Oscillator provides a variable sample rate from once every 3 seconds to once every 100 milliseconds. Provisions for external sample rates up to 25 milliseconds are included.

Anode Strobing circuit pulses each readout tube on for 1.5 ms during the appropriate time period of each complete cycle of the instrument. This means that during every 18 millisecond recycle period of the instrument each readout tube is only on for 1.5 milliseconds.

Sample and Hold circuitry is used during the Measurement cycle of the instrument when the input is sampled and is first digitized.

Logic Section provides the solid state switching commands for both range and function controls.

D. A-D Converter

Inverting Amplifier is used only when the input voltage being measured is negative. When the input to the instrument is positive, FET switches cause the output of the Buffer to bypass the Inverting Amplifier.

Polarity Detector circuitry automatically detects the polarity of the input signal and provides outputs for the logic switching of the Inverting Amplifier.

A-D Amplifier has two fixed gains, and is one of the key elements in the Recirculating Remainder system of analog digital conversion system.

Ladders and Switches provide a voltage back to the summing junction of the A-D Amplifier and also a discrete voltage that is stored in the Analog Storage for use when the instrument is in the Storage Mode of operation.

Sample and Hold circuitry provides storage for the remainder voltages while the instrument is in the Measurement Mode of operation.

Analog Comparitor provides current to the Current Controlled Oscillator whenever the output of the A-D Amplifier exceeds the reference voltage of 7 volts.

Current Controlled Oscillator provides a pulse train whose output pulses are proportional in repitition rate to the current being supplied it. The pulses supplied by this oscillator are fed to the 16 State Binary Counter for decoding.

E. **AC Converter**

The input impedance is 1 megohm into the inverting amplifier. The gain is controlled by feedback switching. Rectification is accomplished by dual section half wave diodes.

Filtering is accomplished by a 3 section RC filter combined with large feedback loop capacitors. The output of the filter is fed to a times 10 Inverting Amplifier which feeds the A-D Converter of the instrument.

F. **Millivolt/Ohms Converter**

In millivolt operation a chopper stabelizer operational amplifier is used which feeds an intergrated circuit operational amplifier with a gain of 10 on the 1000 millivolt scale and a gain of 100 on the 100 millivolt scale. The output of the millivolt section of the converter is 0 to 12 volts DC.

In Ohms operation the converter uses the 7 volt reference to supply current to the unknown resistance and the voltage drop across that resistor is translated by the instrument into ohms values. The instrument input is so configured as to provide modified four terminal resistance measurements for additional accuracy.

G. **External Reference**

This option provides a means of referencing the instrument to external sources from 2 to 10.5 volts via a chopper stabelized operational amplifier to increase the isolation between the system under measurement and the 8300.

H. **Remote Control Unit**

The Remote Control Unit can be operated from either 5 volt logic or from relay closures and will give full control of function and Range of the instrument. Four lines provide control of the range functions and 7 lines provide function control. Light operated diodes give this option the very high degree of isolation required.

I. **Data Output Unit**
Will provide parallel, serial or parallel bit format output. Transformer coupling provides the isolation required. This unit has a high degree of flexibility for properly mating with the broadest variety of configurations.

III. SUB-SECTION FUNCTIONS

A. Power Supplies (Figure 2)

The primary windings are so configured as to provide either 115 VAC or 230 VAC input power which is selected by a switch on the rear panel.

The +18 volt supply is zener regulated and provides the initial reference for the other supplies, so if trouble exists in the +18 supply it is reasonable to expect that all of the other supplies will also show a problem.

The −18 volt supply is referenced to the +18 volt supply by the voltage drop across R231, R223.

The +5 volt supply, which is used for the logic functions is regulated by the voltage drop appearing across the +18 volt supply and R229.

The +7 volt reference supply is regulated by zener pack A1. The voltage to this circuit is fed by the +18 volt supply.

The +190 volt supply for the readout tubes is regulated by a voltage division which is referenced to the +18 volt supply.

B. Logic Section (Logic Schematic)

The Master Clock is a 33 Hz square wave generator and provides the timing for the entire instrument. The pulses from the flip-flop are fed to the clock input of a J-K flip-flop where the F and F pulses are generated. (Pictures A & B)

The F pulse is then applied to Q1 where the H pulse is generated. (Figure 3)

The 6 State Shift Register (Figures 3 & 6) are logic pack 4B generate the six timing pulses used for timing in the instrument. These are the $\overline{\text{ZERO}}$, A, $\overline{\text{A}}$, B, $\overline{\text{B}}$, C, $\overline{\text{C}}$, D, $\overline{\text{D}}$, E, and $\overline{\text{E}}$ pulses which are all clocked to the $\overline{\text{H}}$ pulses. This register is reset by the MS pulse from logic pack 16C at the end of each complete instrument cycle.

The 16 State Binary Counter (Figure 7) translates the pulses from the Current Controlled Oscillator into Binary Coded Decimal (BCD) output and controlls the Ladder Switches and the Decoder Driver. It is reset at the beginning of each time period by the $\overline{\text{H}}$ pulse.

The 9's Catcher operates gate 9B when $\overline{\text{W}}$ and $\overline{\text{Z}}$ and $\overline{\text{A}}$ to stop the Current Controlled Oscillator.

The Conditional 11's Catcher, logic packs 8A and 19B operate to stop the 16 State Binary Counter in the A period.

The 12's Catcher operates in the A period and causes the instrument to up-range and the Over light to turn on.

Current Controlled Oscillator produces a pulse train that is proportional in repitition rate to the current being supplied. The oscillator is stopped in F time. It's output is fed to the 16 State Binary Counter to be translated into BCD output. (Picture D)

Analog Cycle Control provides gating functions that prevent the instrument from recycling until it completes it's present cycle, thus avoiding erronious readings.

Display Circuits consist of the Function Lights, which are 5 volt lamps operated by the logic controls in the instrument and the relays and associated circuitry.

The Anode Strobing Control provides +190 volts to the readout tubes during the last half of each time period and lights each lamp in coordination with the proper time period.

Decoder Driver accepts the BCD output from the 16 State Binary Counter and translates it into decimal output, grounding the appropriate line to the readout tubes so that the tube will light when the +190 volts is applied by the Anode Strobing Control. Q41 operates the first readout tube whenever the count in A period reaches ten.

Manual Range Logic provides first priority of selection to the local front panel switches and provides the range commands as shown in Figure 8. Figure 9 shows the output as fed to the range flip-flop 18a and 18b.

Auto Range Logic operates when W and X from the 16 State Binary Counter and causes $\overline{UP}$ which initiates up ranging in the A period. $\overline{W}$ and $\overline{X}$ and $\overline{Y}$ and $\overline{Z}$ (zero) result in a $\overline{DN}$ signal which initiates down ranging in the A period. In addition when no Filter selection is made the instrument requires a settling time of about 10 ms. This is provided by R40 shunted by R41. When the Filter is selected R40 provides about 230 ms of delay for settling time.

IV. BUFFER BOARD THEORY

The buffer pre-amplifier of the 8300A is basically an inverting unity gain voltage follower. Its primary function is to provide an impedance conversion between the signal source being measured and the A-D Converter input.

Referring to Figure 16, the buffer could be represented as shown. The input resistance of the buffer is $\frac{E_s}{I_s}$ If I_s can be kept small, then the impedance will be high. The resistance R_L is the leakage resistance between the High and Low input termianls. Care was taken in the mechanical design of the instrument so that the leakage resistance would always be greater than 10^{12} ohms.

The other component of I_s is I_e. Elementary feedback theory indicates that the input resistance of an amplifier connected as shown in Figure 16 will be the product of the open loop input resistance and the loop gain. Junction Field Effect J-FETs, are used in the inputs of the buffer, and thus an open loop input resistance of greater than 10^9 ohms is obtained. The loop gain of the buffer is approximately 10^6, so the input resistance of the actual amplifier is greater than 10^{15} ohms, or much greater than the leakage resistance than could be expected at the input terminals.

Using J-FETs also helps keep the insertion current of the buffer preamplifier less than 50 pa. That means that a source resistance of 1 megohm would cause less than 50 μV or ½ digit of offset due to injection current.

The A-D converter has a full scale input of 12 volts, thus requiring a means of reducing input signals greater than 12 volts, if they are to be measured. For that purpose, a 10 megohm attenuator can be placed in front of the buffer when the input exceeds 12V.

The attenuator has two ratios available. One provides a division of 10 and the other provides a ratio of 100. Both are controlled by the front panel switches or the Remote Control Unit. In the 1000 volt range, the divider ratio is 1/100 and in the 100 volt range the ratio is 1/10. In the 10 volt range the input is direct.

The attenuator connection is as shown in Figure 17, with range commands adjacent to each switch. Limiting circuits are provided at the amplifier input, in series with current limiting resistors so that ±1100 volt signals cannot damage the buffer, even in the 10 volt range.

A zeroing circuit (R47) is provided on the buffer for calibration. The excellent zero stability of the FET pair used at the buffer input makes it unnecessary to provide front panel adjustment.

In addition to providing impedance buffering and signal attenuation, the buffer pre-amplifier also can be called upon to filter the input signal. Internal to the amplifier are roll off networks that establish a unity gain frequency of 3 Hz. This roll off of the gain of the buffer provides high frequency filtering by attenuating the AC signals inside the buffer and presenting a reduced version of the AC signal input to the A-D Converter. The frequency characteristics are shown in Figure 18. A notch filter is provided at 60 Hz and three pole response is present above 30 Hz. As the figure shows, for all frequencies above 50 Hz, the rejection of AC signal at the input is greater than 60 db.

Up to now the buffer has been considered as a single block amplifier. A more detailed explanation of circuit operation is in order. The block diagram shown in Figure 19 is complete enough for signal tracing. For illustration, place a positive DC voltage across the HI and LO input terminals.

Since AMP 1 is a high gain operational amplifier with its inverting terminal grounded, any signal at the non-inverting terminal will produce a large in -phase version of that signal at the amplifiers output. AMP 2 is connected inside of its own feedback loop to give a negative gain of about 2.5. When the amplified positive signal at the output of AMP 1 is applied to AMP 2's loop, the result is that the output of AMP 2 is driven negative. The voltage to which the output of AMP 2 is driven is determined solely by the input signal applied and the voltage to which the non-inverting input of AMP 1 is driven. Since the loop gain of the buffer is very high, the positive input of AMP 1 effectively does not change, and as pointed out earlier, the FET input does not allow any current flow from the source. Because there is no voltage present with respect to the analog common at the positive input of AMP 1, and because no current can flow from the source, the output of AMP 2 can only go to $-E_S$ with respect to analog common. Thus, we have an inverting voltage follower.

When FILTER is called with the 8300, large capacitors are placed in the feedback paths of both AMP 1 and AMP 2. In addition, both a notch filter and a low pass filter are placed in the forward gain path. The feedback capacitors force the 3 Hz unity gain bandwidth for the buffer, the notch filter provides 60 Hz filtering, and the low pass filter adds two additional poles at effectively 30 Hz.

V. AC CONVERTER THEORY

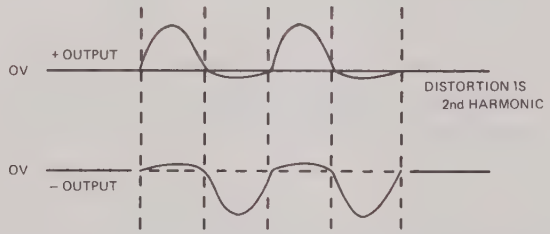
The AC Converter option for the 8300A converts input AC voltages, in four ranges, to DC for measurement by the A-D Converter. The output of the Converter is 0 to 12 VDC , which represents full scale.

Zero adjust for the AC Option is located on the Buffer Board and is accessable from the front panel. Calibration of the assembly is made in the factory prior to shipment and the board may be placed in an instrument, the zero adjustment made and calibration checked. It should not be necessary to recalibrate the option after installation.

The block daigram, (Figure 20) is divided into two major parts. A wide band operational re-

ctifier circuit where the ranging is accomplished and a DC difference (or subtracting) amplifier-intergrator where the rectifier output is filtered and amplified. The DC amplifier also provides the low source impedance required by the A-D Converter.

The operational rectifier circuit consists of an inverting transconductance amplifier and load resistor with feedback around them providing a loop gain of about 5×10^3 at mid band. The feedback is changed for ranging with reed relay switches. The input resistor is 1.11 megohms. This value shunted by the 10 megohm DC input divider is 1 megohm at the 8300A input. Q1 is a FET used as a source follower and Q2 provides a low impedance guard voltage which is used to bootstrap most of the capacity that otherwise would appear from the FET gate to common. The first two differential pairs are in a dual inline package. They and Q4 and Q5 develope the gain. Q3 and Q6 are current sources with such values that clipping due to overload is symmetrical. Changes in capacitor charges will be small and amplifier recovery time minimized. Q7 compensates for capacitance losses in the diodes at low levels. A symmetrical half wave rectifier placed between the amplifier and load resistor develops equal (+) and (–) DC voltages proportional to the amplifier output current. At full scale this current is near 2 mz. The two outputs have the following wave forms.



The DC difference amplifier-integrator filters the waveform and amplifies the DC difference between them by about 10 times for measurement by the A-D Converter. Three section filtering, which cannot be observed on the readout when the input voltage is at full scale and above 100 Hz. Below 100 Hz a few digits respond to the ripple. At 50 Hz the readout excursions do not exceed ±.01% of reading and at 30 Hz are within ±.05% of reading. Q9 is a dual FET which is used for the input of the low drift DC amplifier. Further gain for the DC amplifier is developed by a monolithic operational amplifier to produce a total loop gain at DC of about 5×10^5.

VI. MILLIVOLT/OHMS CONVERTER THEORY

As the name inplies, the Millivolt/Ohms Converter performs two functions. The use of the converter in the 8300A allows measurement of resistance over five ranges and provides two DC voltage ranges in addition to the three ranges offered by the basic instrument. The five resistance ranges are 1 KΩ, 10 KΩ, 100 KΩ, 1000 KΩ and 10 MΩ. The two additional DC voltage ranges are 1000 mv and 100 mv. As with the basic instrument, the above ranges have a 20% over-range capability. Thus the 1 KΩ range will accurately read to 1.19999 KΩ.

This converter can be thought of as two converters. One converter is a chopper amplifier which provides a DC amplification of an unknown voltage prior to A-D Conversion. Signal gain is necessary if a 100 mv signal on the 100 mv range is to provide a corresponding 10V DC signal into the A-D Converter.

The other converter in the Millivolt/Ohms Converter is a precision current ladder which, in conjunction with the Buffer amplifier, provides a known current through the resistor to be measured. Refering to Figure 21, a MOSFET chopper is used across the summing junctions of an operational amplifier. The signal developed due to the chopping action is amplified and presented through a capacitor to a half-wave synchronous demodulator. The Demodulator output is sent to a high gain (at DC) operational amplifier connected as an integrator. The integrator output is brought to the MOSFET chopper in a manner to insure negative feed-back. An input RC network provides input filtering to prevent beat frequency products at the amplifier output and balanced AC impedances for the chopper.

The use of the MOSFET chopper as shown allows the spike developed due to capacitive coupling from gate drive to channel to become a common mode signal for a high common mode rejection operational amplifier. Balanced AC impedances at the chopper provide cancellation effect of the offset current and voltage due to the capacitive spike. The new result is a chopper amplifier capable of operating at a fairly high frequency with small voltage and current offsets, and with spikes of low enough value to keep the AC amplifier from saturating. The above operation is achieved without large adjustments for spike compensation.

The overall millivolt amplifier can be considered to be a high DC gain operational amplifier utilizing potentiometric feedback to provide programmed gains of x10 or x100 and very high input impedance at DC. The A-D Converter follows the millivolt converter to provide digitization of the amplified analog representation of the input signal to the millivolt converter.

The current ladder is connected to the Buffer and the millivolt converter as shown in Figure 22. The inverting terminal of the Buffer amplifier is held very near analog common by the feedback connection of the unknown resistance. Because the inverting terminal is held near ground, and because the input current to the Buffer is small, the current through the unknown resistor is set by the reference voltage (7 volts) and the resistor selected by the range command. For the three upper KΩ ranges, the output of the buffer is presented to the A-D Converter. Thus since the A-D Converter digitizes 11.9999 as full scale, then that voltage must represent full scale on the KΩ ranges. Simple arithmetic shows us that the sampling currents for the three ranges to be 1 us, 10 ua, and 100 ua respectively.

For the 1 KΩ and the 10 KΩ range, smaller full scale voltages are used in order to keep load dissipation down. Thus, on these two ranges, the millivolt converter is used to amplify the voltage across the unknown resistor and present the amplified voltage to the A-D Converter.

In addition to providing smaller full scale impressed voltages in the lower two resistance ranges, the use of the millivolt converter allows a "modified four terminal" resistance measurement to be made. The term "modified four terminal" is used because the technique employed requires a small current in one of the sense lines that would not be present in a true four terminal resistance measurement. The sense current magnitude is determined by the voltage impressed on the resistor to be measured divided by R_i. By example, if the sense line resistance is 10Ω, then the error due to the sense current can be computed roughly as follows:

$$\text{Error} = \frac{10\Omega}{R_i} = \frac{100\Omega}{1000\Omega} = 10^{-4} \text{ or } 100 \text{ ppm of reading.}$$

If a two terminal reading were made at the 1 KΩ level with a 10Ω resistance in the hook-up wires, the error would be about 10,000 ppm. The improvement in performance using a "modified four terminal" measurement is obvious.

VII. EXTERNAL REFERENCE THEORY

The 8300A input terminal for VDC measurements is the input to the A-D Converter and therefore, will have a maximum voltage of ±12v with respect to the instrument common, Figure 23. Since it may be necessary to connect the common of the input to the common of External Reference input and the External Reference output common is instrument common, a means of isolating the commons becomes necessary.

Refer to Figure 24. Switches S1 and S2 are arranged so that when one set is closed, the other is open. S1 is closing during a non-critical (the A-D ZERO time) portion of the measurement cycle and allowed to charge to the voltage, E_R. When S2 is closed, the output of A_1 goes to E_R satisfying the voltage follower.

Refering to the circuit schematic, A2 is the S1 of the block diagram, Q4 and Q5 the switch, S2. A matched pair of J-FETS followed by a monolithic amplifier made up the high input impedance voltage follower. Q8 and R17 is a constant current source for the J-FET amplifiers. Frequency compensation is provided by the C4, C5 and C6.

The reference voltage is sensed through R18 from the A-D Amplifier board compensating for line drops. Low sense (Reference Common) also comes from the main board. CR7 and CR8 provide feedback to the voltage follower when the reed relay, S1 is open, keeping the amplifier output within 0.5v of the voltage of C8 to control the gate drive for Q4.

C7 forms an RC filter with the input driver giving improved noise performance. C9 provides an input impedance to the voltage follower during the time the FET switches, Q5 and Q6 are open.

Q1 and Q2 are gate drivers for the J-FET switches. Using the reference voltage for the collector supply of Q2 assures that the gate signal of Q4 never goes positive with respect to its terminal. The gate of Q5 is clamped to within .2v of common by diode CR6. R13 limits the current through CR6. C2 compensates for the capacity of CR6.

A voltage of as much as ±12.0v with respect to reference common will appear at the low terminal of EX REF input when the EX REF common is tied to the instrument input common.

A schematic showing the voltage distribution is shown in Figure 25. The MOS FET's used are P-channel enhancement mode devices. A negative gate voltage of 10v or more is needed to insure that the transistor is on. 0v or a positive gate voltage turns the transistor off. Refering to Figure 25, the upper switch needs a minimum of −15v to turn on and a maximum of 19v to turn off. The bottom switch needs a minimum of −22v to turn on and a maximum of 12v to turn off.

The MOS FET gate driver is redrawn in Figure 26 showing the peak voltages. When the transistor is saturated, CR1 is back biased. When the transistor is cutoff, C3 charges to 8v because of the 12v drop across the zener. This voltage subtracts from the collector voltage giving the voltage shown.

When the EXT REF control line is 5v (the EXT REF button pushed) −18v is applied to the local Disable line with Q10 and Q12.

Input protection is provided with CR4, CR5 and R12.

VIII. RECIRCULATING REMAINDER ANALOG TO DIGITAL CONVERSION (Figures 10, 11 and Schematics)

Refering to Figure 3 the time relationships can more easily be visualized. The Master clock generates a 333 Hz square wave, which is fed to the clock input of a J-K flip-flop, 3F, which produces the F and F pulses. The F pulse is further modified by Q1 where the H pulse is generated. The H pulses are fed to the clock inputs of the 6 State Shift Register, where five of the six timing pulses are generated. The sixth, $\overline{\text{ZERO}}$ pulse is generated by the action of the NAND gate 4B. Note that it is possible to divide any of the time periods into two equal parts by using the F and/or the F pulses. (These time periods are refered to as A1, A2, B1, B2 . . . etc.)

During the ZERO time period the $\overline{\text{ZERO}}$ pulse operates the A-D Auto Zero Drive Circuit. Q118 conducts and connects the output of A2 to the zero holding capacitor C115 and at the same time the input of the amplifier is grounded. This operation places the offset of A2 across C115 and effectively removes it for the remainder of the cycle. A similar circuit removes the offset from the Inverting Amplifier during "C" period of time.

For the purposes of illustration, it is necessary to make several assumptions and specify several conditions. The assumption is made that ranging functions are complete and that a voltage of –6.3524 volts is appearing at the input to the main chassis. (R102) The instrument is entering a Measurement Cycle.

The –6.3524 volts is amplified and inverted by the Inverting Amplifier and appears at the Polarity Detector which is enabled by Gate 4 pulse. The voltage is now positive due to the action of the Inverting Amplifier. The positive output to the Polarity Detector will cause the Polarity Detector to turn the plus gate Q112 on. This will cause the negative input to R102 to move directly to the input of the A-D Amplifier through R166. (In the case just taken the input to the instrument would have been positive. Had the input been negative, the Polarity Detector would have turned on the Minus gate, Q111 and the incoming signal would have been inverted by the Inverting Amplifier. This output is fed to the A-D Amplifier through R165.

NOTE: The inverting amplifier is used only when the input to the 8300A is negative.

The negative voltage appearing at the inverting input to the A-D Amplifier will cause a positive voltage to appear at its output. When the output of the A-D Amplifier exceed the 7.0 volt reference, the Analog Comparitor will produce current. This current is fed to the Current Controlled Oscillator (CCO). The Current Controlled Oscillator will produce a pulse train whose repitition rate is proportional to the current being supplied. These pulses are fed to the 16 State Binary Counter where they are translated into Binary Coded Decimal (BCD) output. The BCD output is connected to the Ladder Driver circuits and with each incremental increase of digit value the ladders will produce a current step. When the Primary Ladder has been caused to step 6 times the output from the Ladder being fed back to the input of the A-D Amplifier will cause the amplifier to satisfy itself with an output of less than 7 volts. At this time the Analog Comparitor will no longer supply current to the Current Controlled Oscillator and no further pulses will be generated. The remainder voltage that appeared at the output of the A-D Amplifier to satisfy it is now applied to capacitor C118 through Q125 which was enabled by the Gate 2 pulse (Sample and Hold)

The secondary Ladder output is fed to capacitor C110 in Display Storage. The BCD output of the 16 State Binary Counter is also fed to the Decoder Driver, where it is decimalized, which will cause ground potential to appear on the "6" line to all readout tubes. The A pulse and the

F pulse are fed into the Anode Strobing Control which will cause the +190 volts to be pulsed on during the last half of the A time period, thus causing the "6" to be displayed by the first read-out tube.

At the beginning of the B time period the $\bar{H}$ pulse will reset the 16 State Binary Counter. The Gate 1 & 22 pulse will enable Sample and Hold transistors Q124 and Q127. The remainder voltage stored on capacitor C108 is now applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and again the Analog Comparitor will produce current, which is fed to the Current Controlled Oscillator. The oscillator pulses are counted by the 16 State Binary Counter and converted to BCD. The Ladders are caused to increase their output incrimentally with each pulse until the Primary Ladder feeds a "3" pulse back to the summing junction of the A-D Amplifier. At this time the output of the amplifier is less than 7 volts which causes the Analog Comparitor to stop the current flow to the Current Controlled Oscillator. Etc. The remainder voltage appearing at the output of the A-D Amplifier is applied to capacitor C109 in the Sample and Hold circuit through Q127. The Secondary Ladder output is stored on Display Storage capacitor C111 through Q129 and Q147.

Again the Decoder Driver has caused a ground potential to appear on all of the "3" lines to the Readout tubes and the F pulse through CR105 and the B pulse through Q34 will cause the +190 volts to be applied to the second readout tube, where the digit "3" will be displayed.

The process continues using alternately capacitors C108 and C109 in the Sample and Hold circuit to store the remainders and then reapply them to the summing junction of the A-D Amplifier. As each time period digit is developed, the Secondary Ladder stores its output on seccessive capacitors in the Display Storage capacitors C110 through C114.

It is well to remember that the above description was of a Measure Cycle. All of the digits were developed using the Sample and Hold circuit. The following description is of the Storage Cycle.

Gate pulse 4 is the primary control over the determination of whether the 8300A will enter a Measure Cycle or a Storage Cycle. If Gate 4 pulse is not present the Polarity Detector will not be activated and the instrument will continue in Storage Cycle. Gate 4 pulse is generated by Q116 and will only be present in A period when an M signal is present.

Since in this example we are entering a Storage cycle no Gate 4 signal will be present and Q146 in the Display storage will be enabled. The last Measurement Cycle left incremental voltages stored in the Display Storage capacitors C110 through C114 that correspond to the digits 63524.

During the A period Q128 and Q146 will be enabled allowing the voltage stored in C110 to be applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and the Analog Comparitor will supply current to the Current Controlled Oscillator. The oscillator will generate a series of pulses causing the 16 State Binary Counter to translate the pulses into BCD output. The BCD output will cause the Ladders to switch until the Primary Ladder output satisfies the A-D Amplifier feedback. At this point in time the output from the amplifier will be below 7 volts and the Analog Comparitor will no longer supply current to the CCO. The pulses stop and the output of the Secondary Ladder will again be stored in capacitor C110 in the Display Storage circuit. The BCD 6 from the 16 State Binary Counter will drive the Decoder Driver which will produce a ground potential on all of the "6" leads to the readout tubes. The combination of A and F pulses will cause Q35 and Q40 to apply +190 volts to the anode of V1 which will light the "6".

During the B period, Q129 and Q147 will be enabled, applying the voltage stored in C111 to be applied to the summing junction of the A-D Amplifier. The output of the A-D Amplifier will

exceed the 7.0 volt reference and the analog comparitor will supply current to the Current Controlled Oscillator. The pulses from the CCO will be counted and translated to BCD output by the 16 State Binary Counter.

The BCD output being applied to the Ladder Driver Circuits will cause the ladders to increase their outputs until the output of the Primary Ladder, which is fed back to the summing junction of the A-D Amplifier satisfies the amplifier. At this point in time the output of the amplifier will be below the 7.0 volt reference and the Analog Comparitor will no longer furnish current to the CCO and the pulses will stop. Since a "3" was digitized and stored in the Display Storage for this time period, a three from the Primary Ladder will cause the A-D Amplifier to be satisfied. The output of the Secondary Ladder will be stored in the Display Storage during the last half of the time period and the "3" will be displayed by V2 during the last half of the time period by the operation of the Anode Strobing Control.

Each increment of voltage stored in the Display Storage will be digitized and re-stored in the Display Storage circuit until all five digits have been displayed. At the end of the Storage Cycle if no Measure pulse has been generated prior to A time the 8300A will again enter a Storage Cycle. This process will repeat until a Measure pulse is generated, prior to A time and then at A time a Gate 4 pulse will be generated and the instrument will again sample the input voltage and enter a Measurement Cycle.

IX. TROUBLESHOOTING AND ANALYSIS

1. The following is a list of recommended test equipment that is required to test and calibrate the the 8300A. If the recommended equipment is not available, other equipment which meets the required specifications may be used.

EQUIPMENT NOMENCLATURE	RECOMMENDED EQUIPMENT
Oscilloscope	Tektronix Model 547
Oscilloscope Plug-In	Tektronix Model 1A1
Oscilloscope Probes	Tektronix Model P6010
DC Voltage Source	Fluke Model 343A DC Voltage Calibrator
AC Voltage Source	HP Model 745A
Differential Voltmeter	Fluke Model 885A

2. An excellent source of synchronization for the Oscilloscope may be obtained by using the $\overline{\text{ZERO}}$ signal that is available at TP4 or TP108. By proper adjustment of the horizontal trace time it is possible to see all of the other timing pulses in their proper relationship.
3. With the covers and shields removed it is reasonable to expect to see more noise in the output as the 8300A is quite sensitive to interference when these protections are removed.
4. Figure 30 gives the general location of the various sections of the instrument.
5. Figure 29 locates the various test points (TP) and is a guide to the location and index of the logic packs.
6. All voltage measurements and pulse observations should be made with reference to the instrument signal ground which is available at TP3 and TP109.
7. Figure 27 gives a step by step procedure for troubleshooting the Display section of the 8300A.
8. Figure 28 gives an excellent step by step procedure for troubleshooting the analog circuitry.
9. Many cases of trouble can be analized from the operation and readout observations of the instrument. As examples the following are presented:

   a. Readout is in error only in the negative polarity.

      It is reasonable to assume that the trouble is located in either the polarity FET switch-or in the Inverting Amplifier since these paths are utilized only in the negative polarity.

   b. More than one digit displayed in the readout tubes.

      The Decoder Driver is the most likely source of this trouble. If ground potential is supplied to more than one of the decimal lines to the readout tubes, multiple numbers will light. There remains the possibility that the Anode Strobing circuits are mal-functioning.

c. Only the first digit is displayed, all others read 0.

It is reasonable to assume that the remainders are not being stored in the Sample and Hold circuitry. This can be caused by a failure in the FET switches or a short in the storage capacitors. It is also possible that two significant digits will be developed and displayed.

d. First digit reads higher than the input voltage and all other digits read 0.

Count the pulses from the Current Controlled Oscillator. If correct check the BCD output of the A4 Counter. If the BCD output is correct the Ladder output voltage could be too high.

e. A large signal of either polarity is needed to cause a reading of other than 0.0000.

The A-D Auto Zeroing circuit, Q117 and Q118 should be checked.

f. None of the readout tubes lighted.

Check the +5 and the +190 volt supplied.

10. The basic instrument may be checked by applying a 0 to 12 volt DC signal at the input to the Inverting Amplifier. This should cause the instrument to display the voltage applied.

11. By applying a jumper between TP6 and TP201 the instrument can be made to sample continuiously. This procedure can be used to locate trouble in the Storage circuitry.

12. The logic section of the instrument can be broken up into several independent sections for trouble analysis as follows:

a. Master Clock

Check the output of Q45, then look for the F, $\overline{H}$ and $\overline{ZERO}$ pulses.

b. Six State Shift Register.

Check for the presence of the A, B, C, D, and E pulses and their inversions.

c. Check the output of the Current Controlled Oscillator and the BCD output of the 16 State Binary Counter.

d. Display readout tubes.

Anodes and Anode Strobing circuitry.
Cathode circuits including the Decoder Driver.
Decimal lines.

e. Function Indicators.

+5 volt incandescent lights and associated circuitry.

f. Sample Oscillator should be checked for output.

g. Figures C through G and the Picture waveforms attached will be of additional assistance in locating troubles.

X. DATA OUTPUT UNIT

The Data Output Unit Option is felt to be included in a minority of cases, this section will include the theory of operation and the troubleshooting and analysis.

A. General

The Data Output Unit (DOU) receives DVM measurement data through guarded pulse transformers and by means of appropriate control circuitry, enters this data into a self-contained, random access digital memory. Outputs are available in positive logic, BCD 1-2-4-8 parallel format. A strobing operation, which produces a parallel bit, serial-character format may be easily implimented by connecting outputs together in groups, as desired, and manipulating gate inputs. (See DOU Block Diagram, Figure 40)

A system of output blanking is incorporated which has a threefold purpose. First, it holds all outputs in an OFF state any time the DVM is performing a measurement or is in the digitizing process. It is during these periods that the DOU memory is being loaded and if the outputs were turned on, transient, meaningless data would be momentarily displayed. Secondly, signal conditioner settling time is automatically considered by a circuit called the Programmed One-Shot (POS). The POS ensures that the user obtains rated accuracy data in the minimum possible time, reguardless of the function performed, by holding outputs off or blanked until valid data is obtainable. The POS holds outputs OFF just long enough for the signal conditioner in use to settle to rated accuracy. When a different signal conditioner is called into operation by the user, the POS automatically adjusts timeout delay to the new conditions. At timeout, the POS triggers a new measurement before turning on the outputs 23 milliseconds later. Thirdly, automatic ranging is detected by the DOU, and data outputs are blanked during ranging functions. After blanking is complete, the outputs will remain ON and unchanged until the DVM is again commanded to sample.

The following is an example of a typical sequence of internal events as initiated by the user generated sample command:

a. An unknown input and a trigger pulse (command to sample) are applied to the DVM.

b. The POS reverts to its unstable state, thereby inhibiting all outputs.

c. The DVM makes a preliminary measurement (requiring 6 milliseconds) to determine if ranging is necessary.

d. Autoranging takes place and the timeout is increased by 250 milliseconds for each range change.

e. The programmed one-shot begins to time out in accordance with the function delay data registered in the DOU memory.

f. At the end of the required settling time, the DVM is automatically commanded to sample again by the POS as it reverts to its stable state.

g. New data is registered in the DOU memory as a result of this final sample.

h. All the outputs are then turned ON to provide function, range, polarity and the specified accuracy numerical data. A ready flag indicates whether outputs are on or off.

B. Logic Notation

A description of the logic symbology used in the DOU is given in Figure 40. A J-K flip-flop that is in the "1" condition or is set "high" has a high output from the Q terminal.

The orientation of the flip-flops in the schematics is the same as the flip-flop shown in Figure 40.. This method of notation enables input/output terminals of the flip-flops to be identified without the necessity of redundant lettering of each device symbol. In the main, the routing of logic and control signal on the schematics is accomplished without connecting lines, which greatly reduces conjestion. The routing of the memory outputs within the DOU is given by numerical designations. For example, 16-P3, which appears at pin 2 of output buffer gate 3A, refers to pin 3 of shift register 16.

C. **Multiplexers**

The DVM function, range and polarity inputs are applied to dual multiplexer circuitry consisting of transistors Q14 through Q20 and NAND gates 28A, 28B and 28D (see DOU schematic). The five gates comprising each multiplexer are enabled sequentially by the 6 State Shift Register signals. The multiplexer outputs are applied to trigger circuits consisting of NOR gates 27A through 27D and transformers T1 and T2. The pulses produced by T1 and T2 secondaries are applied to RS flip-flops composed of inverters 13B. 13C, 13E and 13F which reconstruct the multiplexer inputs for application to the data gates. Examples of the RS flip-flop outputs are shown in the timing diagram of Figure 41. (Signals ⑨ and ⑩) and correspond to the following DVM functions and input conditions: VDC function with filter, 100 range and positive voltage applied to the input. A complete list of waveforms appearing at the output of the RS flip-flops is given in the troubleshooting section of the manual.

D. **Digits Counter**

The digits counter consists of J-K flip-flops 26W, 26X, 25Y and 25Z. The input flip-flop 25Z is toggled by positive pulses, which are transferred through the guard by transistor Q13 and transformer T3. The counter produces a 4 bit binary output that is entered into the memory via the data gates. The counter is reset at the beginning of each su-period of the measurement cycle by the $\overline{F}$ signal. The W', Y', and Z' counter outputs are also applied to NAND gate 22A, which stops the counter at a count of "11" and generates a high at the input of flip-flop 21L. If another pulse appears at the secondary of T3, it is indicative of "12" in the first decade (i.e. instrument overload). The 12th pulse toggles flip-flop 21L to produce an overload indication at the DOU output, pin 35B.

E. **Data Gates**

The data gates consist of NAND gates 22B, 23A through 23C and 24A through 24D. The gates are controlled by F', F', S and S signals so that the 10 bits function, range and polarity data and 20 bits of numerical data are presented to the shift register memory at the proper times. These data bits are loaded in accordance with the load sequence. (Figure 42) and are steered by these data gates.

F. **Random Access Memory**

The DOU memory is composed of shift registers 10, 12, 14 and 16. Data is loaded serially into the shift registers. The loading sequence is controlled by clock pulses, which are produced by gates 15A through 15D, gate 19D and associated circuitry. Steering signals S and S together with the loading signal F', develop loading pulses as shown in Figure 43. NAND gate 19D inverter 13A and associated circuitry delay the F' signal for approximately 10 microseconds so that all data present at the shift register inputs will be stabelized before clocking occurs.

G. Control

F′ and $\overline{F'}$ signals are produced by an RF flip-flop consisting of NOR gates 19A, 19B and associated circuitry. The trigger for the flip-flop is developed by gates 29A through 29C and transformer T4. The F′ and $\overline{F'}$ signals are conditioned by the $\overline{F}$. $\overline{M}$ and $\overline{ZERO}$ signals so that the F′ and $\overline{F'}$ signals occur only during periods A through E of the DVM measurement cycle. The steering flip-flop is triggered by the F′ signal and produces S and $\overline{S}$ signals.

The $\overline{S}$ output of the steering flip-flop is applied to transistor Q9 and associated components, which comprise a rechargable one-shot. This circuit is responsible for initializing control circuit conditions and providing for generation of the M signal. The sequence of operation of the one-shot and associated circuitry is as follows: (Control timing signals are shown in Figure 43.)

a. Measurement cycle is initiated.

b. RS flip-flop 19A, 19B are set to "1" condition. (Pin 2 of 19A high)

c. Flip-flop 20B is reset by $\overline{F'}$.

d. Overload flip-flop 21L is reset by a measurement inclusion signal generated at pin 9 of flip-flop 20B.

e. Measure/Store flip-flop (20A) is set by overload reset signal. (Signal No. 4)

f. Gate 17C is inhibited, thereby inhibiting all output buffer gates.

g. The steering flip-flop is toggled (middle of "A" period) and capacitor C14 begins to charge toward +5v.

h. The steering flip-flop is again toggled (middle of "B" period) and capacitor C14 is quickly discharged to 0.9v.

i. Steps (f) and (g) repeat for "C", "D" and "E" periods.

j. Following "E" period, C14 continues to charge until Q9 tis turned on.

k. Q8 then turns on and sets the overload reset flip-flop (20B) and the steering flip-flop (21S).

l. The Measure/Store flip-flop is reset by a negative trigger developed in the circuit of Q7.

m. The output buffer gates are enabled and the data becomes available.

In addition to providing a pesudo Measure/Store signal, the circuit of flip-flop 20A and transistor Q7 also function as an autorange detector Control signal timing under autorange conditions is shown in Figure 43.. If the decision to autorange is made, (middle of "A" period), the DVM logic places the instrument in storage mode. This locks out the F signal in the DOU control circuit and, consequently, no pulses are produced in T4 secondary, excepting the first. With no F′ signal to toggle filp-flop 21S, the rechargable one-shot times out and sets the overload reset flip-flop to the "1" condition. The resulting signal (signal N.2) is applied as a reset pulse to Q7, however, because capacitor C15 has not had time to discharge sufficiently, the trigger threshold of flip-flop 20A is not reached and the flip-flop remains in its previous state. Thus, the output buffer gates are inhibited during the autorange operation. If the instrument had not autoranged, C14 would have acquired sufficient charge during the measurement cycle to enable flip-flop 20A to be triggered, as shown in the timing diagram of Figure 43.

The programmed one-shot consists of NOR gates 18A and 18B, transistors Q3 through Q6, capacitors C9 and associated programming resistors. In its stable state, gate 18A output is high and gate 18B is low. Assume that an external trigger is applied to pin 34 of connector B. The trigger enables gate 18C, thereby triggering the DVM to initiate a measurement cycle. The trigger also enables gate 18A, and the POS then switches to its unstable state. When the POS switches states, the output of gate 19C goes low, resulting in gates 17C being inhibited, Inhibiting gate 17C causes all of the output data buffer gates to be inhibited.

The timeout of POS delay is initiated as soon as the circuit is triggered, i.e., when the POS is triggered, switch Q3 is turned off and C9 begins to charge through the programming network to +5 volts. Delay time is controlled by the memory, which selects resistor R19, R20, R21 or R22, depending on the selected DVM function. When C9 has accumulated sufficient charge, transistors Q4 and Q5 are connected to operate like an SCR, turn on, applying a positive pulse to the input gate 18B through capacitor C24. The POS switches back to its stable state and retriggers the DVM for a final measurement.

The POS is automatically retriggered if the DVM autoranges as a result of the final measurement. For example, if a step voltage were applied to the DVM in mvDC mode, the DVM[logic might not make an autorange decision before the measurement caused by POS to time out. If this occurs, NOR gate 18C goes high, retriggering the POS and initiating a second delay. All autorange operations that are to occur do so at this time. Termination of the second POS delay causes yet another measurement. All settling times have been considered at this time, this measurement is the last and upon completion, 23 milliseconds later, outputs are turned on and data becomes available.

In VDC mode without the FILTER function called, transistor Q6 is enabled. This programs the POS for fastest timeout and clamps pin 9 of gate 18D so that the DVM will not be retriggered by POS timeout.

DATA OUTPUT UNIT TROUBLE ANALYSIS

Trouble analysis of the Data Output Unit is most effeciently performed by a systematic sequence through the unit beginning at the malfunctioning output(s) and working progressively backwards. As familiarity with the unit increases the operator will discover he can shorten the process by skipping obviouse irrelevant steps.

In any analysis certain decisions and/or conclusions must be made. Consult Figure "A" for the suggested decision sequence. Figure "B" is a table which should help to determine how to make the decisions.

FIGURE""B" DECISION AIDS

Example No. 1 DOU Outputs or Reader Faulty?

This decision must be based upon a point-by-point measurement of DOU outputs at points of origin. Many short-cuts are available depending upon the nature of the reader. Suppose all decades except the third are producing correct numbers. The third decade generates the following table:

8300 PANEL	READER PANEL	
00000	00400	CONSIDER: An open in the cable from the DOU to the reader (probably pin 26B DOU connector.) This is the "4" line of the 1-2-4-8 four line BCD code.
11111	11511	
22222	22622	
33333	33733	
44444	44444	
55555	55555	
66666	66666	
77777	77777	
88888	88288	
99999	99399	

Example No. 2

8300 PANEL	READER PANEL	
00000	08000	CONSIDER: An open DOU to reader (probably pin 9A DOU output connector.)
11111	19111	
22222	21222	
44444	42444	
88888	88888	

Example No. 3 Reader panel is 155555, DC+, MV, AC, K, M, EX REF, FLT

The above display remaining regardless of 8300 panel.

Check: Pin 32B DOU Connector. If not 0 to 0.5 VDC, disconnect reader and measure again. If now 0 to 0.5 VDC, reader is at fault, if not look for the problem in the DOU circuit.

NOTE: The forgoing examples assume a reader with full overranging in each decade. Other overrange patterns will not defeat the analysis if the pattern is known.

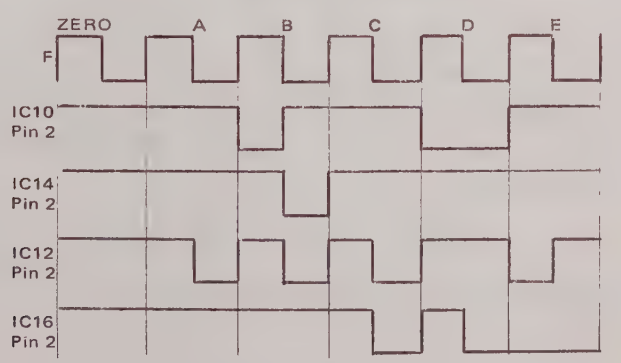
Example No. 4 DOU Memory contains correct data?

It is assumed here that data outputs were determined faulty. This is a static test. Set the 8300 stimulious to produce the trouble analysis information desired. Command to sample once and no more. Using a VTVM, check the data in shift registers (DOU memory) 10, 12, 14, and 16. Use chart of Figure X-4 for location of data. All data in this memory is inverted phase (e.g. 6 would normally be 0110; it is in the memory as 1001.) The chart of Figure X-4 will prove to be a valuable tool for several areas of the DOU circuit.

If the data in the memory is correct, the problem must be in an output buffer gate or in the 1st decade binary to BCD converter I/C 11. If not, it must be determined whether a shift register is faulty. This is proven by determining that serial data input signals are correct and that load signals are correct.

Example No. 5 DOU Memory input data correct?

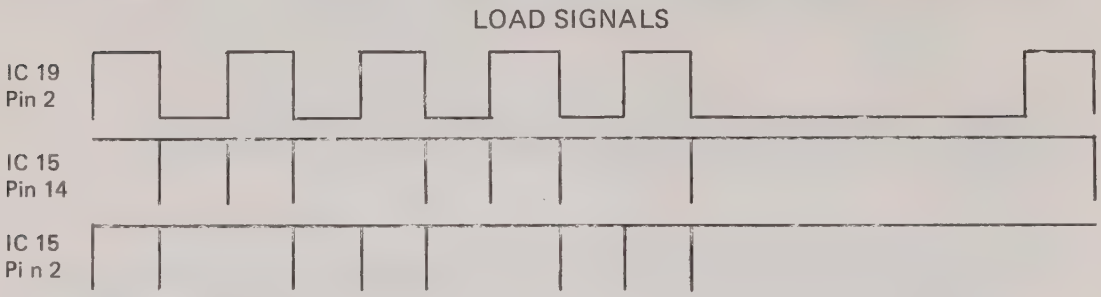
Unfortunately, this must be determined with a dynamic test and for the uninitiated may require observation of a properly operating unit. Set stimulous equipment (8300 & input source) for desired trouble analysis information. Set internal sample command pot on the 8300 to ext position and externally trigger the instrument. The rate should be 25 pps for good scope displays. Ignore reader display as it is unimportant at this time. Sync the scope with the F signal and observe shift register data inputs. Refer to the wave-shape index (Figure "D" reference point no. 9) and index (Figure "E" reference point no. 10). These waveforms are multiplexed with numerical data from the counter and inverted by registration gates I/C 22, 23, 24. Study the schematic and Figures X-4, D, and E to visualize what appearance these signals should have for various combinations of data. A table is not given as there would be 256 possible patterns. It is easier to figure out what a particular combination should produce and will require only a few seconds for an experienced operator using Figure 43. Again remember the inverted phase.



Example: 26.391 VDC FILTERED

Example No. 6 DOU load commands correct?

Refer to the figure below. Use the same set-up as in Example No. 5. A dual trace scope is useful.



If the load commands are correct then something may be wrong with the operation of one of the shift registers. It should be considered (if replacement does not solve the problem) that one of the shift register outputs may be shorted.

Example No. 7 Are the multiplier outputs correct?

Use the same set-up as in Example No. 5. Figures "D" and "E" give tables which illustrate all possible waveforms at I/C 3 Pin 6 and I/C 13 Pin 10 respectively. If the waveforms are correct registration gates I/C 22, 23, 24 may be faulty.

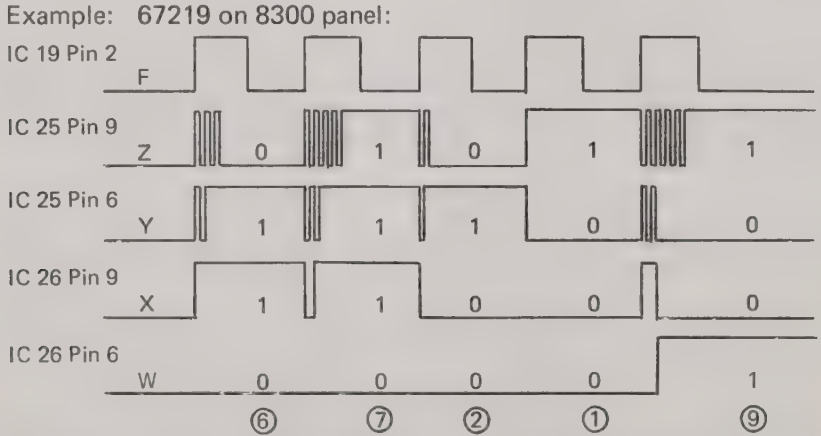
Example No. 8 Are counter jumpers installed?

With the reader connected, check continually between the following points:

23A and 3A 20A and 4A 21A and 1A 22A and 2A	DOU OUTPUT CONNECTOR	IC 25 pin 9 & IC 24 pin 13 IC 25 pin 6 & IC 24 pin 1 IC 26 pin 9 & IC 24 pin 4 IC 26 pin 6 & IC 24 pin 10	Convenient Alternate Locations

Example No. 9 Are the counter outputs correct?

Use the same set-up as in Example No. 5. Consider counter outputs only during second half of each subperiod as below:

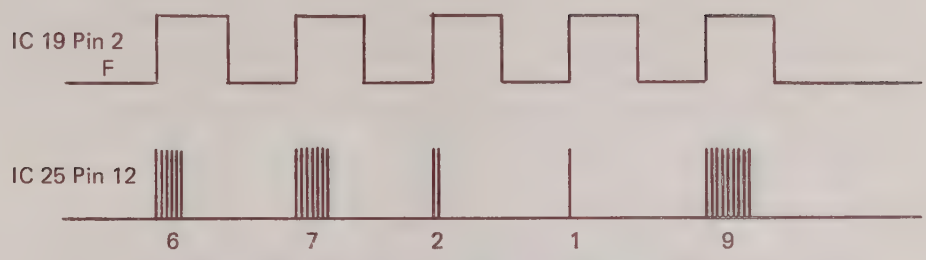


Again, correct counter operation is indicative of a problem in registration gates IC's 22, 23, 24.

Example No. 10 Is counter input correct?

Use the same set-up as in Example No. 5.

Example: 62719



Correct input but incorrect outputs are indicative of counter malfunction.

Example No. 11 Are signals correct at I/C No. 27 pins 3 and 13?

DOU circuit is inside the guard. Therefore the scope must be synced on a signal inside the guard. Use $\overline{\text{ZERO}}$ signal at TP 4 and Common TP3. If multiplexer outputs (test of example 7) are incorrect but observations of example 11 are normal, the transformer circuits of T1 or T2 may be faulty. Signals at pins 3 and 13 of I/C 27 should have waveforms like figures D and E respectively. If not, multiplexers may be at fault or wires broken between DOU input terminals and the counnector inside the guard box.

Example No. 12 Data, Ready or Overload problem?

This is a static test. Command the 8300 to sample only once and then observe, Rate pot on front panel is in external position. If numerals range, polarity or function data is faulty it will be observed on the reader (monitor). If the reader is either blank or displaying 1555.55 VDC+, FILT, MV AC, KΩ, MΩ, EX REF., then the ready line is probably high. The overload display should coincide with a numeral display of 119999 and will be visable on the reader.

Example No. 13 M or P.O.S. problem?

Command to sample only once. Rate pot on the front panel should be in the external position. Check I/C 19 Pin 12 for 0 to 0.5v (P.O.S.) and I/C 17 Pin 17 for 3.5 to 4.5v ($\overline{\text{M}}$ signal). If the $\overline{\text{M}}$ is low it is likely that P.O.S. will be high, but the cause will be $\overline{\text{M}}$ from the control circuit; If $\overline{\text{M}}$ is normal but P.O.S. is high, the programmed one-shot is faulty.

Example No. 14 Are P.O.S. jumpers installed?

Visually check to insure that jumpers 1 & 2 are installed or jumper 1 or 2 and R50 in accordance with delay length table. This is a factory installation so this part of the trouble analysis procedure applies only to factory check-out.

XI. REMOTE CONTROL UNIT

A. General

The RCU functional block diagram is given in Figure 44. . The input function and range commands are applied to circuitry which provides logical interlocking, so that the RCU will respond only to acceptable command combinations. The range and function commands are applied to the photodetectors inside the guard chassis via the light emitting diodes (LED's). The resulting signal is applied to the switches, which activate the DVM control lines.

B. Circuit Description

Input functions and range commands, consisting of switch closures or zero volts DC, are applied to the inverters. The inverter outputs are applied to NAND gates, which provide logic interlocking and drive the light emitting diodes, CR1 through CR11.

The logical interlocking is such that the instrument will respond to the first call received and will ignore succeeding erroneous calls until the first call is released. For example; if KΩ function were called, gate 7B would be enabled, which would inhibit gates 4A, 7A, 3A, 3B and 4B, thereby preventing EXT REF, VDC, MVDC, VAC and 10 MΩ functions from being called.

The detector circuitry consists of phototransistors Q1 through Q11, which detect and amplify the LED outputs. The output of the phototransistors is applied to the output switches and their drivers, transistors Q12 through Q29. The phototransistors and switches are enabled by the remote function and remote range busses, which supply +5 volts DC to the circuitry when the remote switches are pressed.

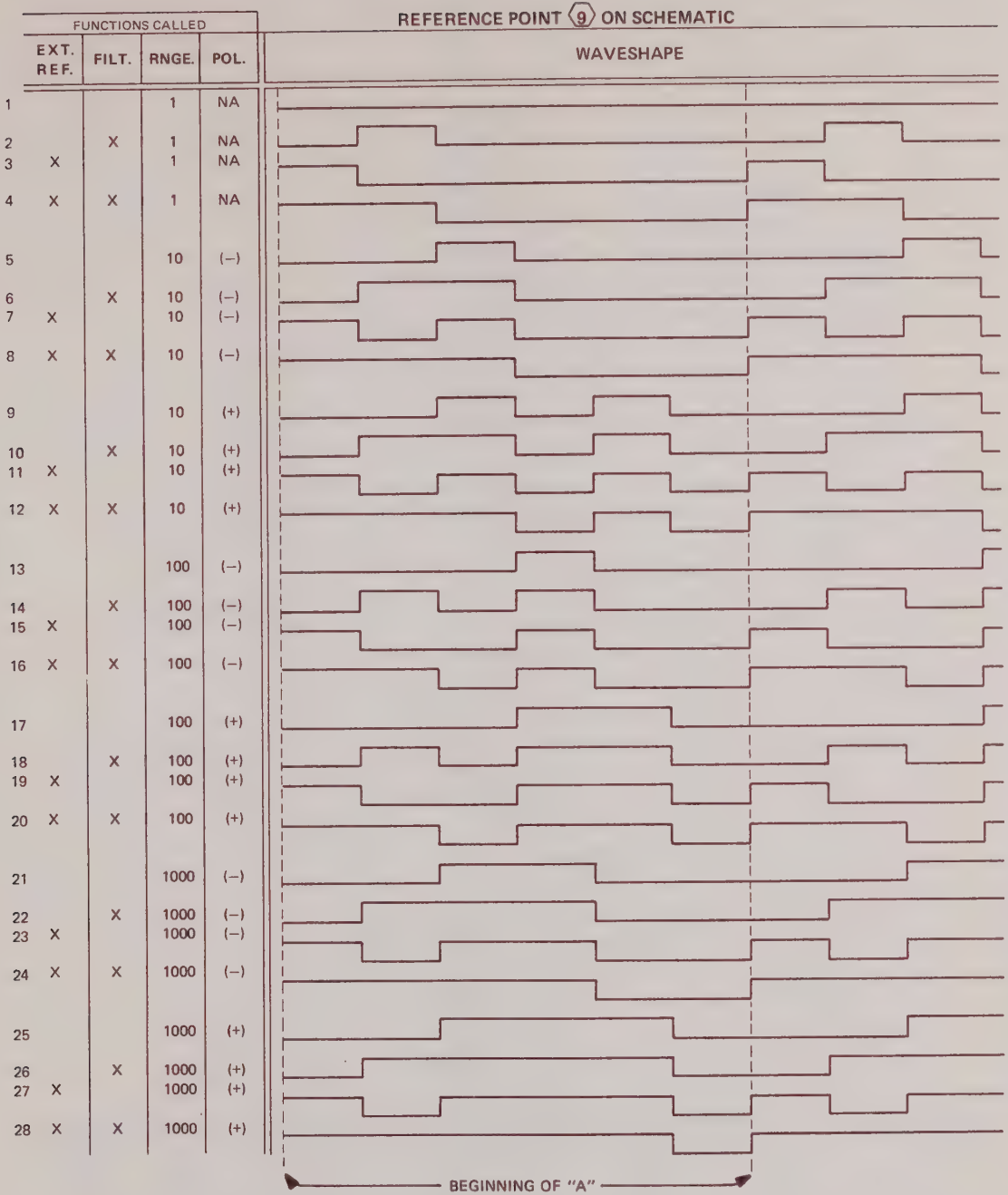


Figure "D"

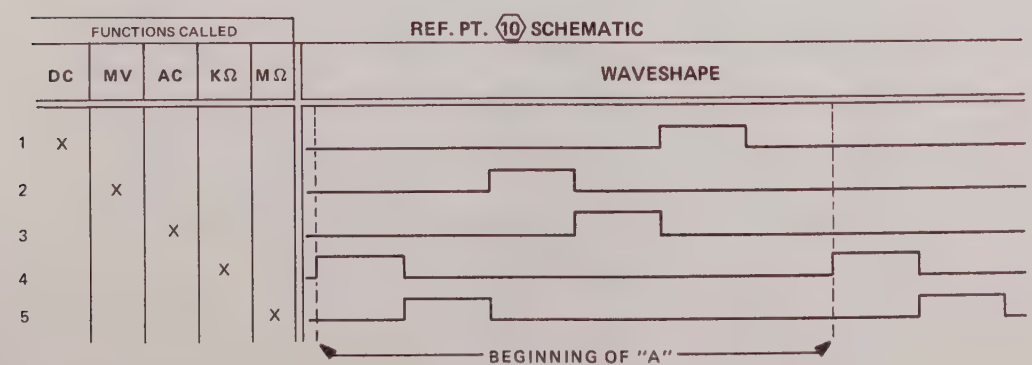


Figure "E"

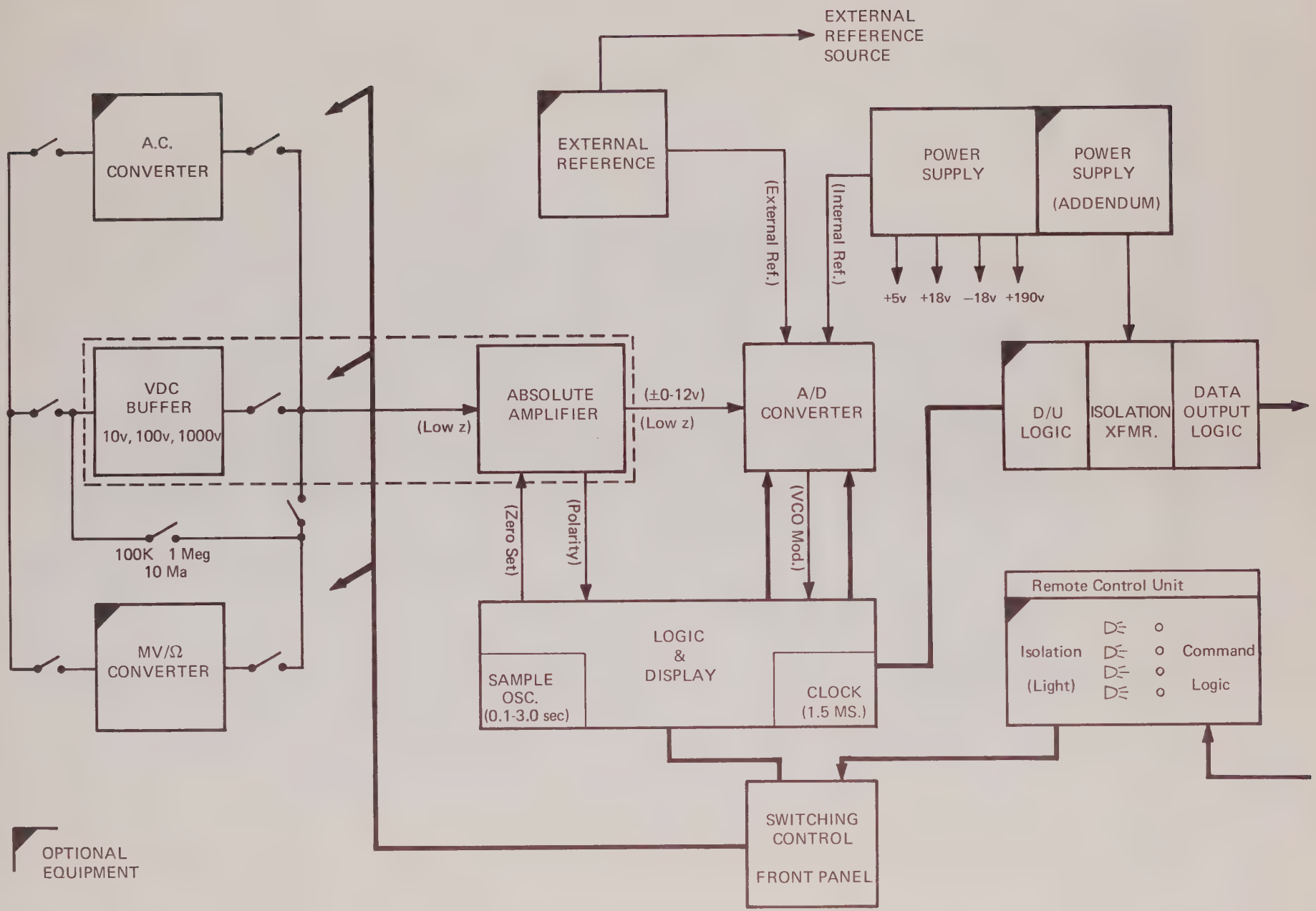


Figure 1. BASIC BLOCK DIAGRAM

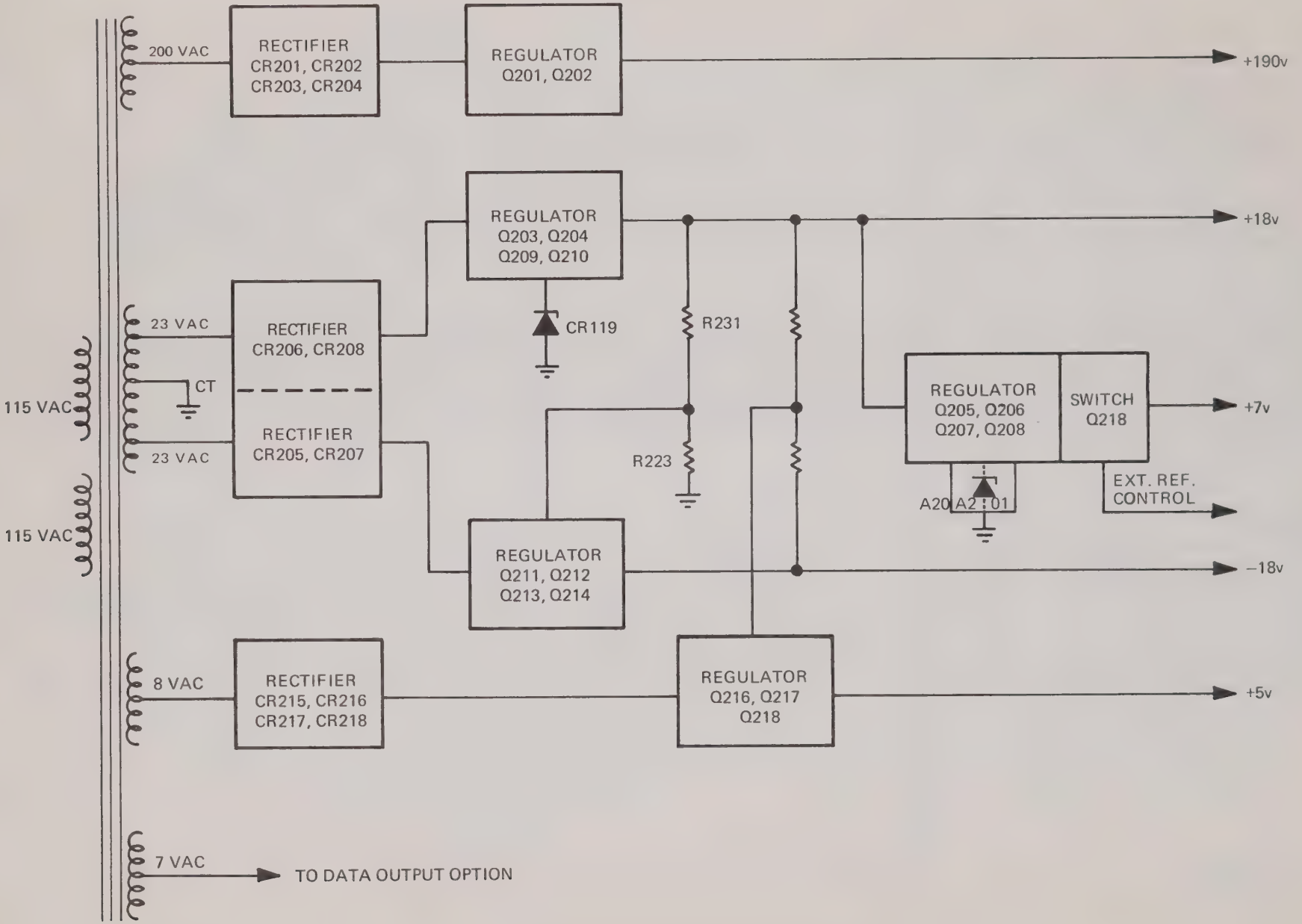


Figure 2. 8300A POWER SUPPLY

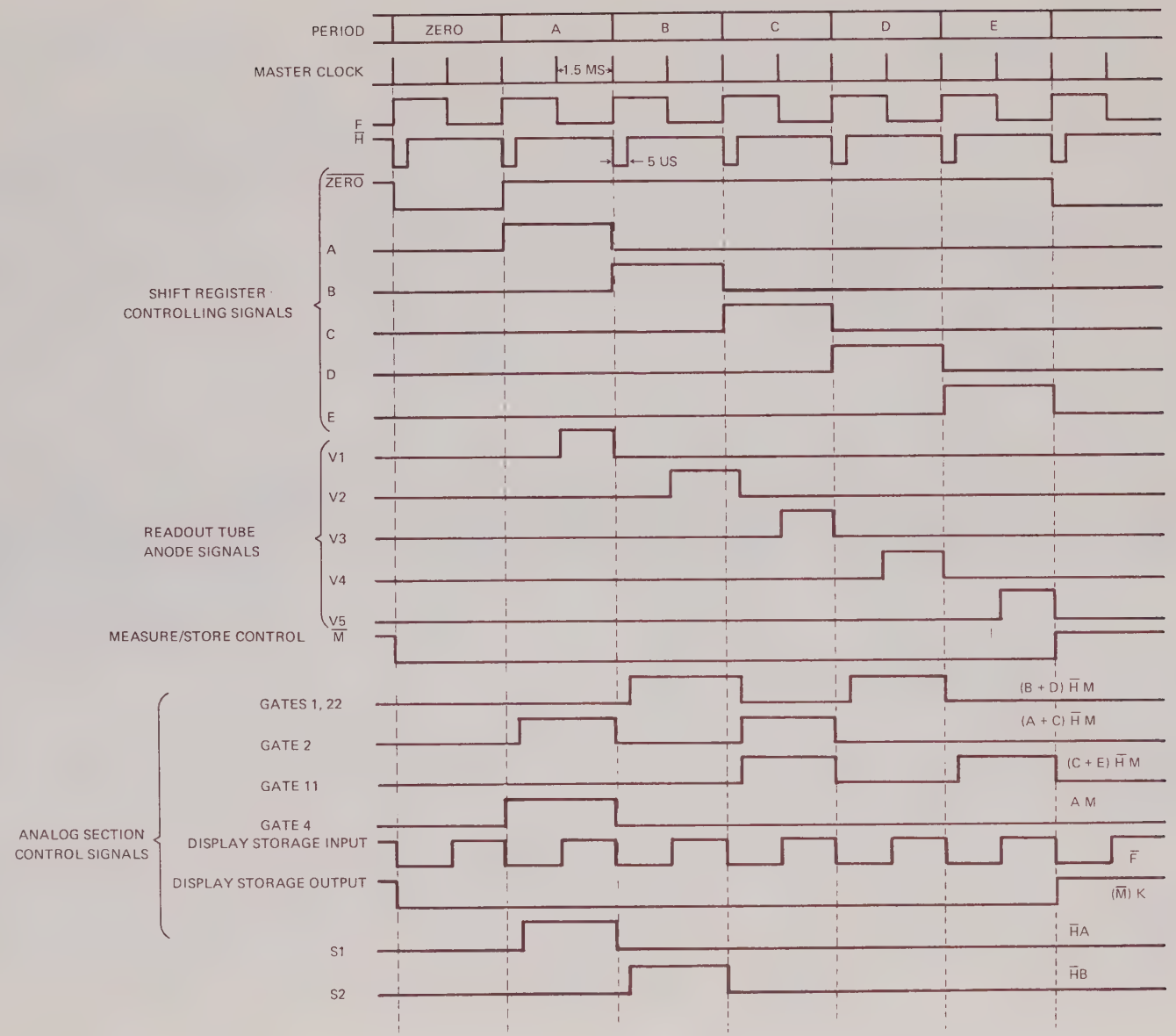


Figure 3. MEASUREMENT CYCLE TIME RELATIONS

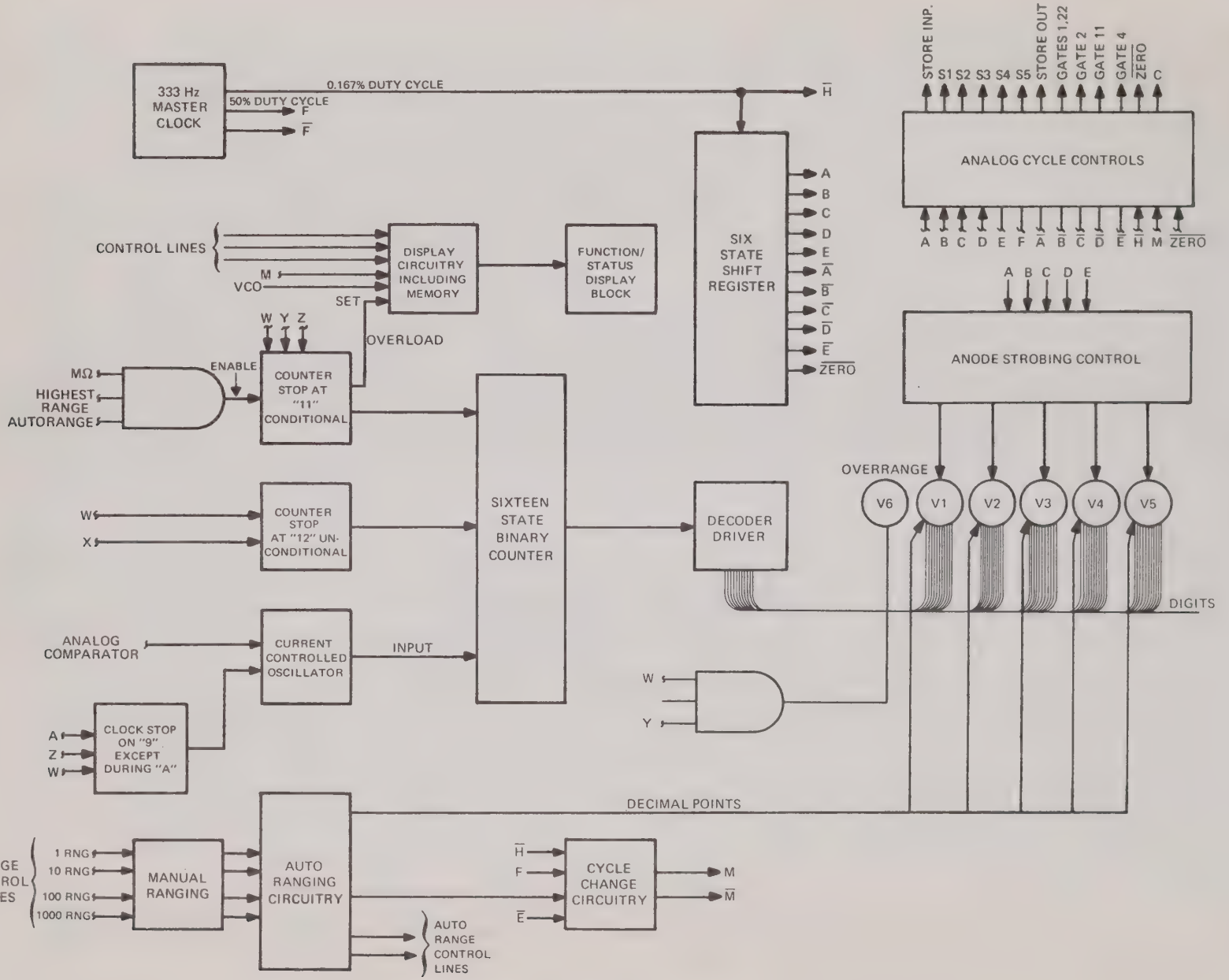


Figure 4. DVM LOGIC AND CONTROL

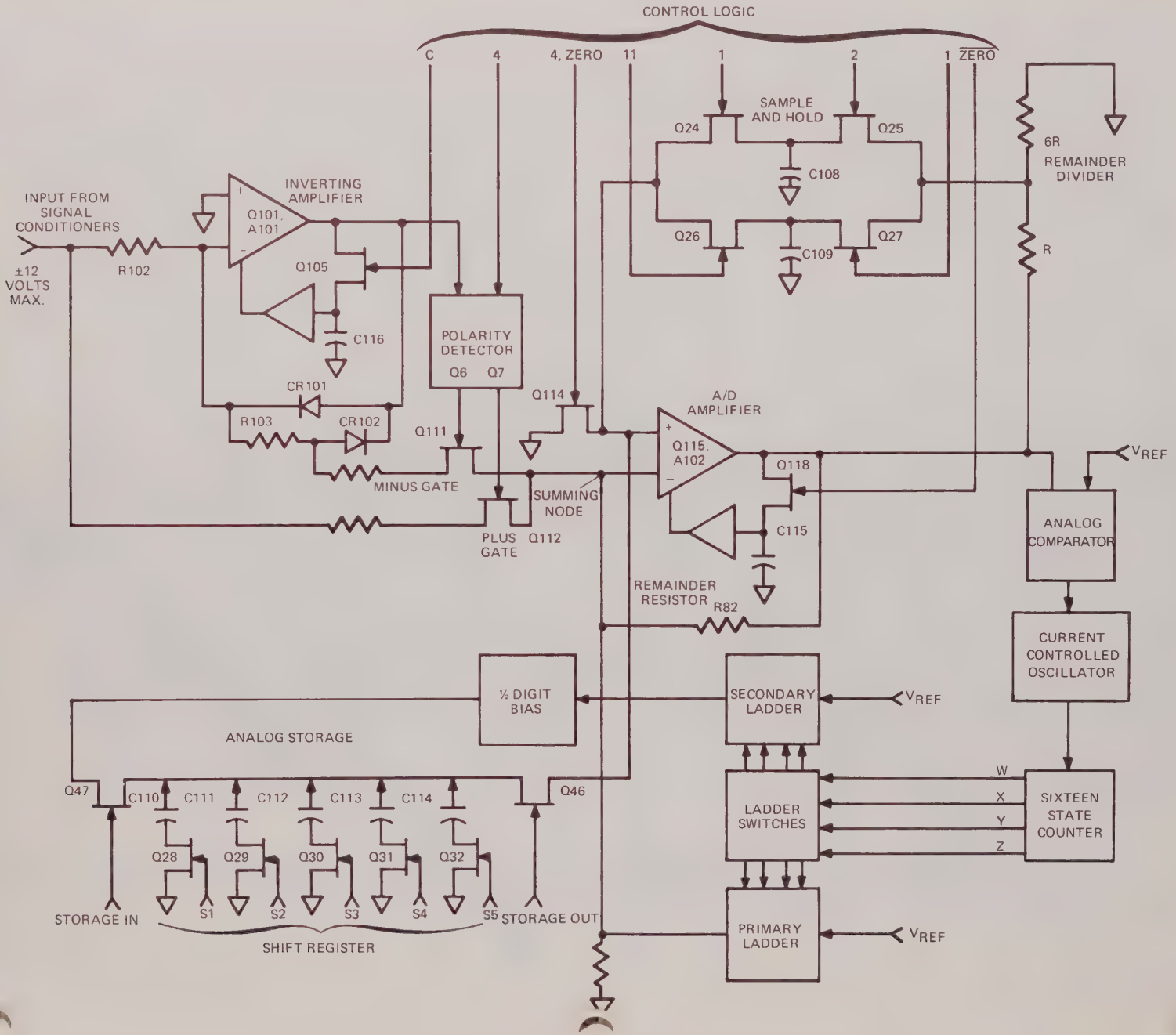


Figure 10. 8300A BLOCK DIAGRAM

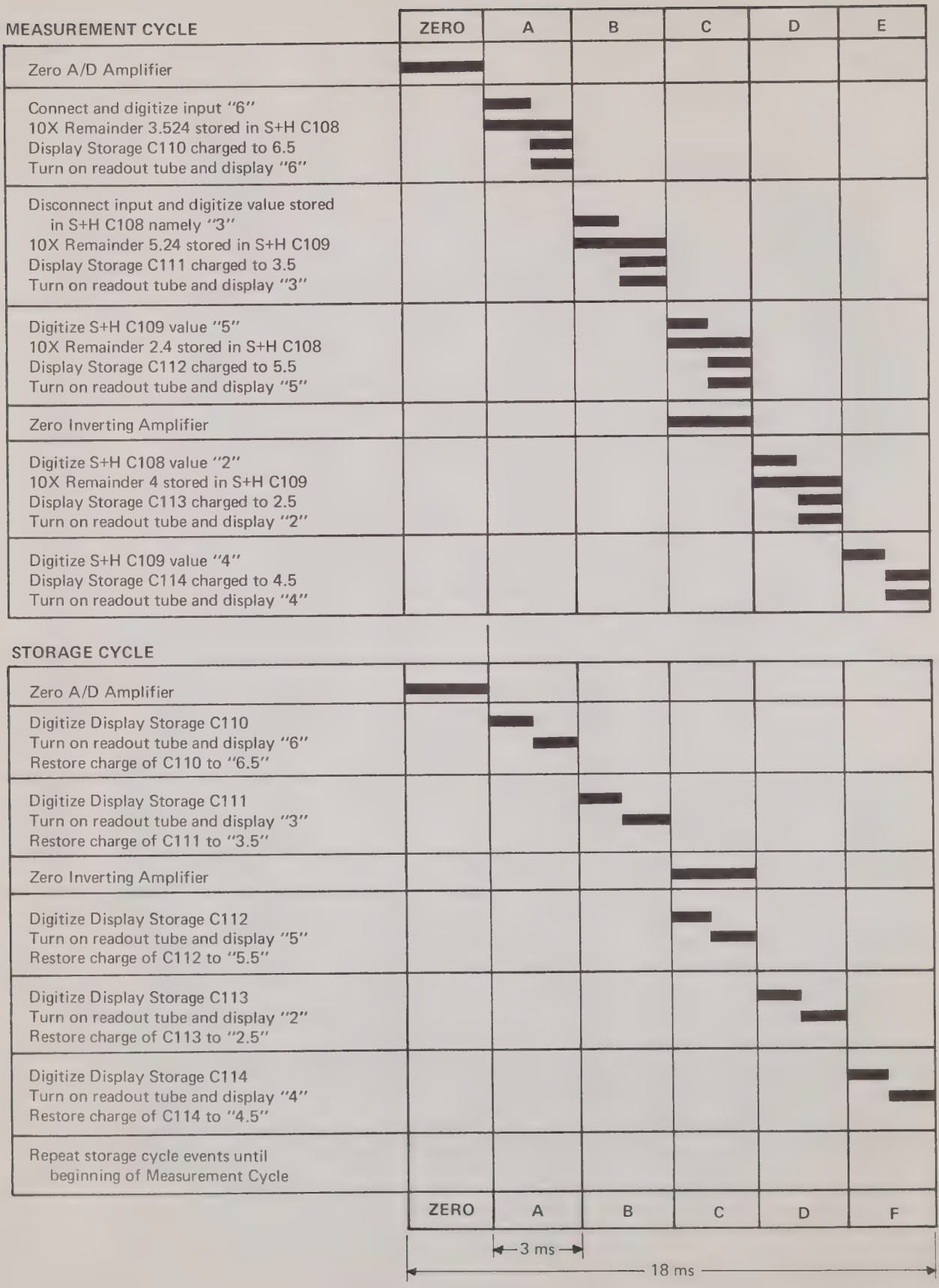
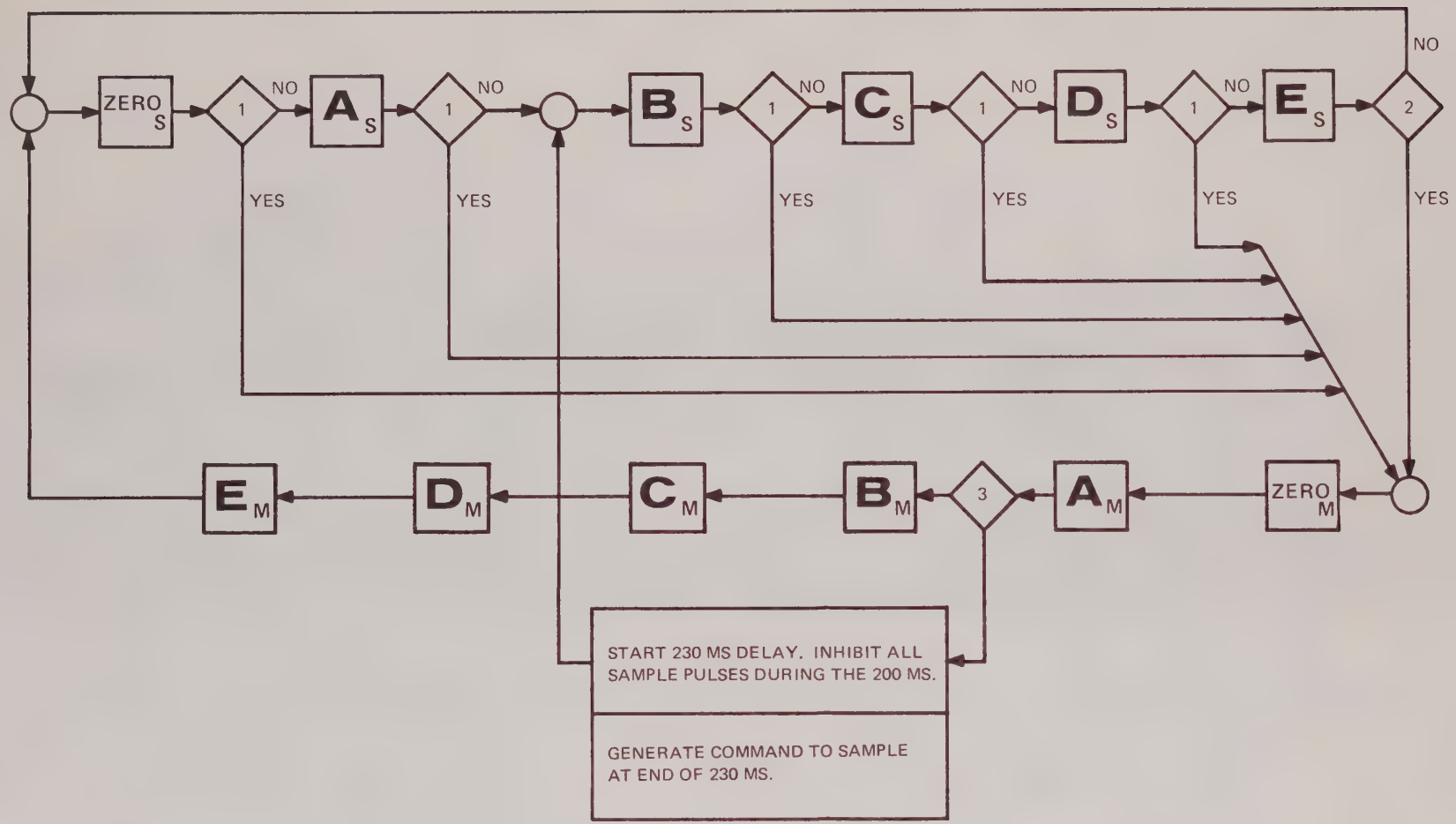

MEASUREMENT CYCLE
ZERO
A
B
C
D
E
Zero A/D Amplifier
Connect and digitize input "6"
10X Remainder 3.524 stored in S+H C108
Display Storage C110 charged to 6.5
Turn on readout tube and display "6"
Disconnect input and digitize value stored in S+H C108 namely "3"
10X Remainder 5.24 stored in S+H C109
Display Storage C111 charged to 3.5
Turn on readout tube and display "3"
Digitize S+H C109 value "5"
10X Remainder 2.4 stored in S+H C108
Display Storage C112 charged to 5.5
Turn on readout tube and display "5"
Zero Inverting Amplifier
Digitize S+H C108 value "2"
10X Remainder 4 stored in S+H C109
Display Storage C113 charged to 2.5
Turn on readout tube and display "2"
Digitize S+H C109 value "4"
Display Storage C114 charged to 4.5
Turn on readout tube and display "4"
STORAGE CYCLE
Zero A/D Amplifier
Digitize Display Storage C110
Turn on readout tube and display "6"
Restore charge of C110 to "6.5"
Digitize Display Storage C111
Turn on readout tube and display "3"
Restore charge of C111 to "3.5"
Zero Inverting Amplifier
Digitize Display Storage C112
Turn on readout tube and display "5"
Restore charge of C112 to "5.5"
Digitize Display Storage C113
Turn on readout tube and display "2"
Restore charge of C113 to "2.5"
Digitize Display Storage C114
Turn on readout tube and display "4"
Restore charge of C114 to "4.5"
Repeat storage cycle events until beginning of Measurement Cycle
ZERO
A
B
C
D
F
3 ms
18 ms

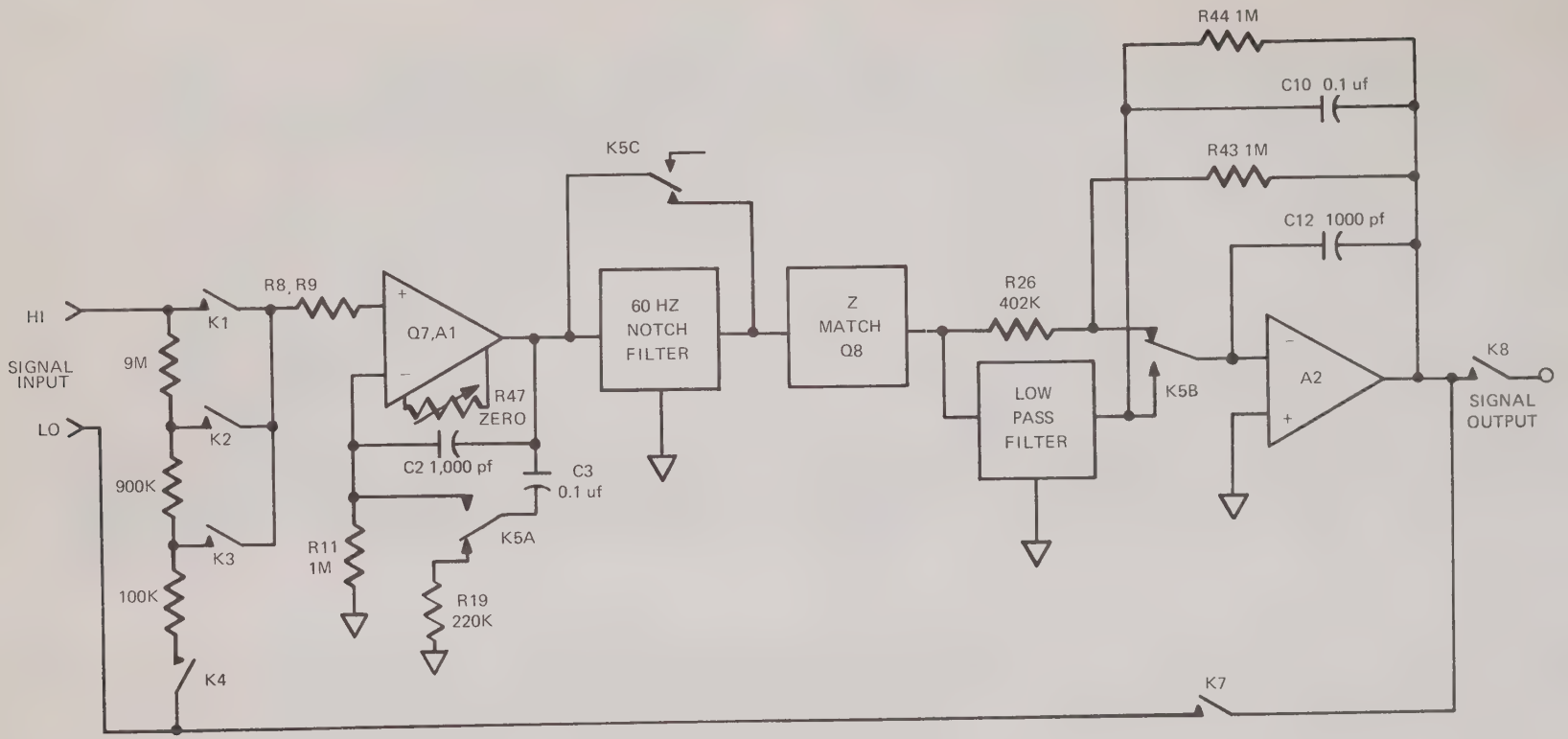
Figure 11.

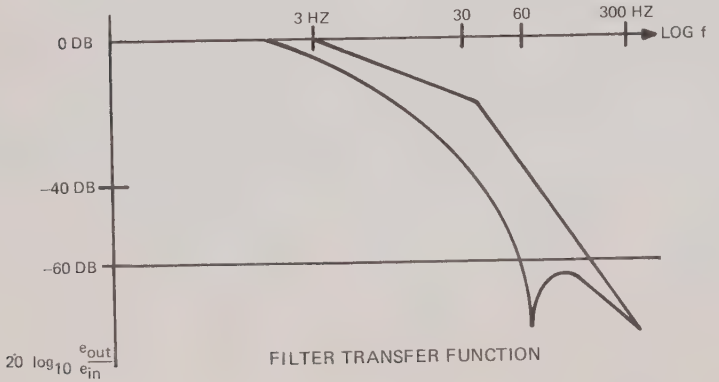


LEGEND:

- ○ RE-ENTRY PATH
- □ 3 MS OPERATION AS INDICATED.
- ◇1 SAMPLE COMMAND RECEIVED DURING PRECEEDING BLOCK AND SAMPLE RATE CONTROL SET TO EXT POSITION.
- ◇2 SAMPLE COMMAND RECEIVED DURING PRECEEDING BLOCK.
- ◇3 REQUIREMENT TO RANGE DETECTED DURING A_M BLOCK.

Figure 12. CYCLE CHANGE FLOW CHART





FILTER TRANSFER FUNCTION

RELAY OPERATION

K1		All KΩ Ranges
		MΩ
		10 VDC
K2	-	100 VDC
K3	-	1000 VDC
		AC
K4		100 VDC
		1000 VDC
K5		Filter and any KΩ, MΩ or DCV
K7		All KΩ, MΩ and DC
K8		All DC, MΩ, 1000 KΩ and 100 KΩ

Figure 13. BUFFER ASSEMBLY BLOCK DIAGRAM

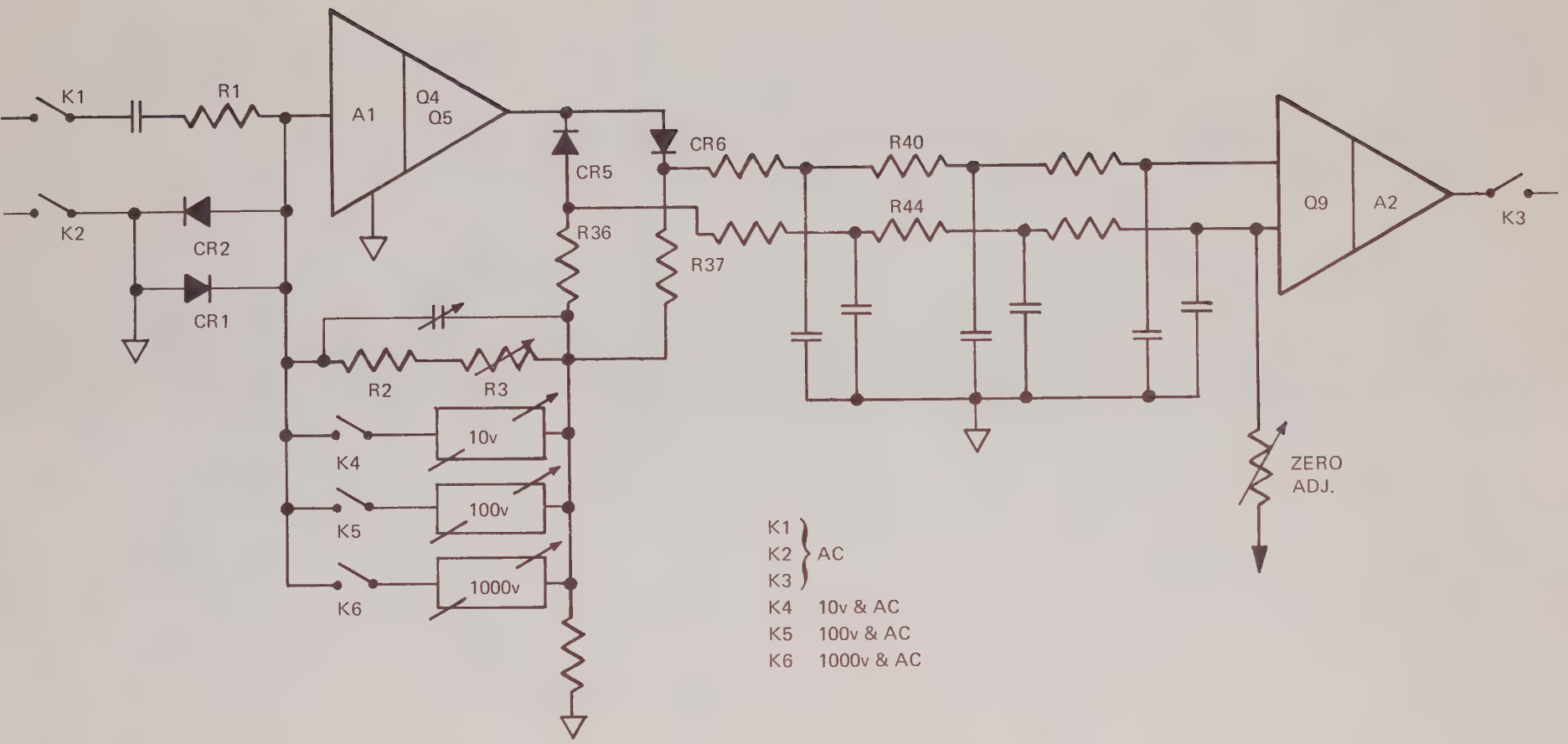
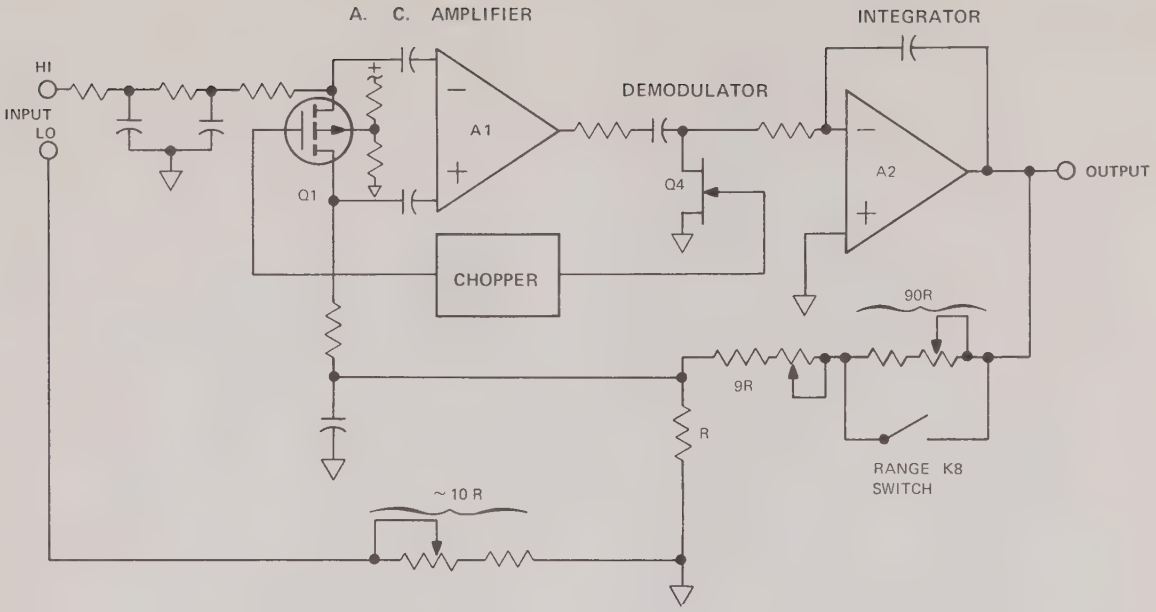
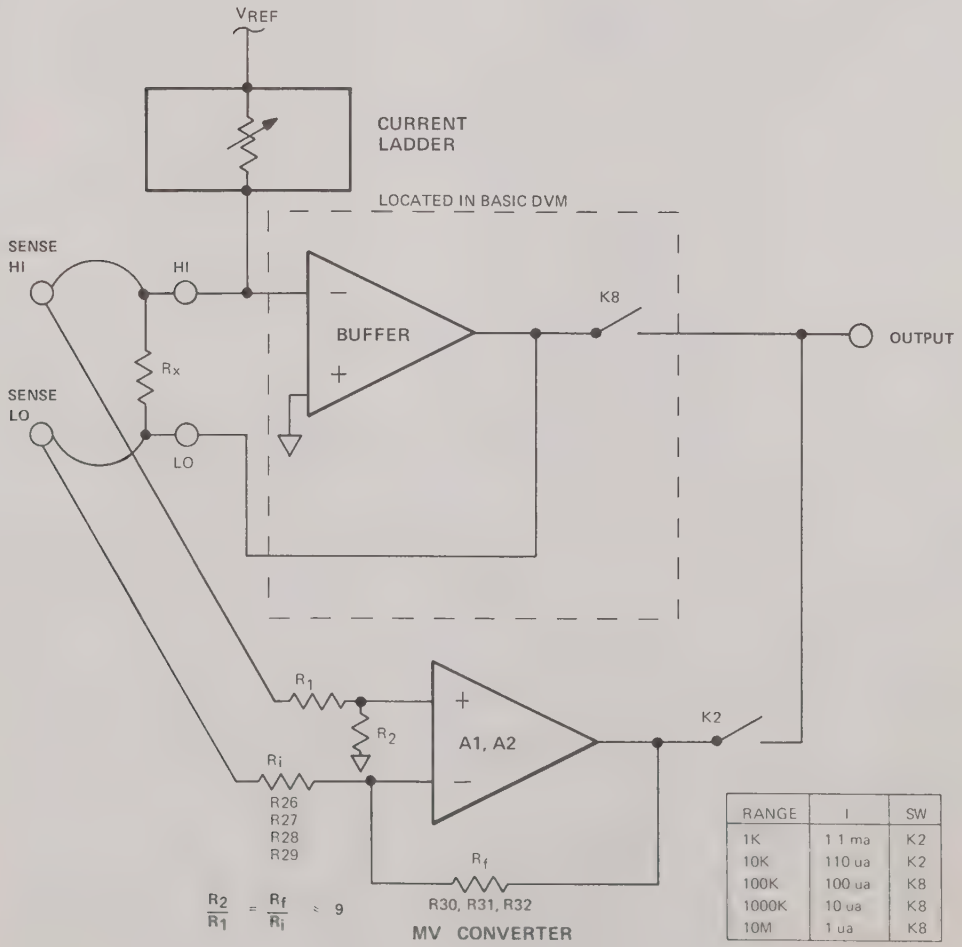


Figure 14. AC CONVERTER OPTION





RANGE	I	SW
1K	1 1 ma	K2
10K	110 ua	K2
100K	100 ua	K8
1000K	10 ua	K8
10M	1 ua	K8

Figure 15.

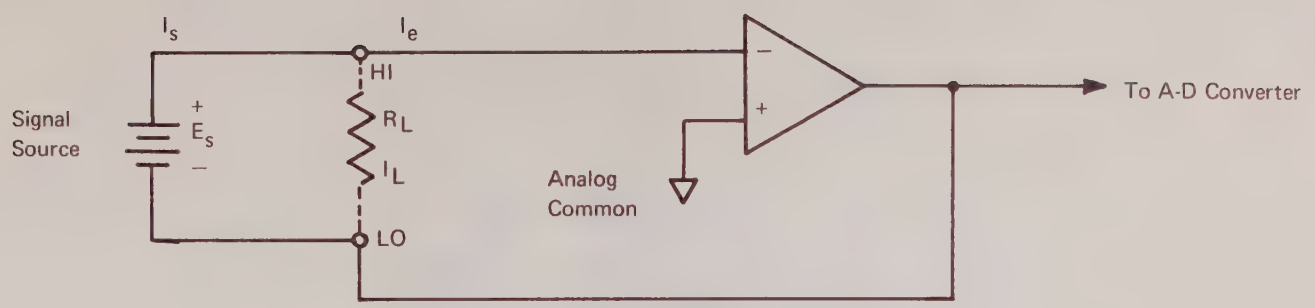


Figure 16. BUFFER

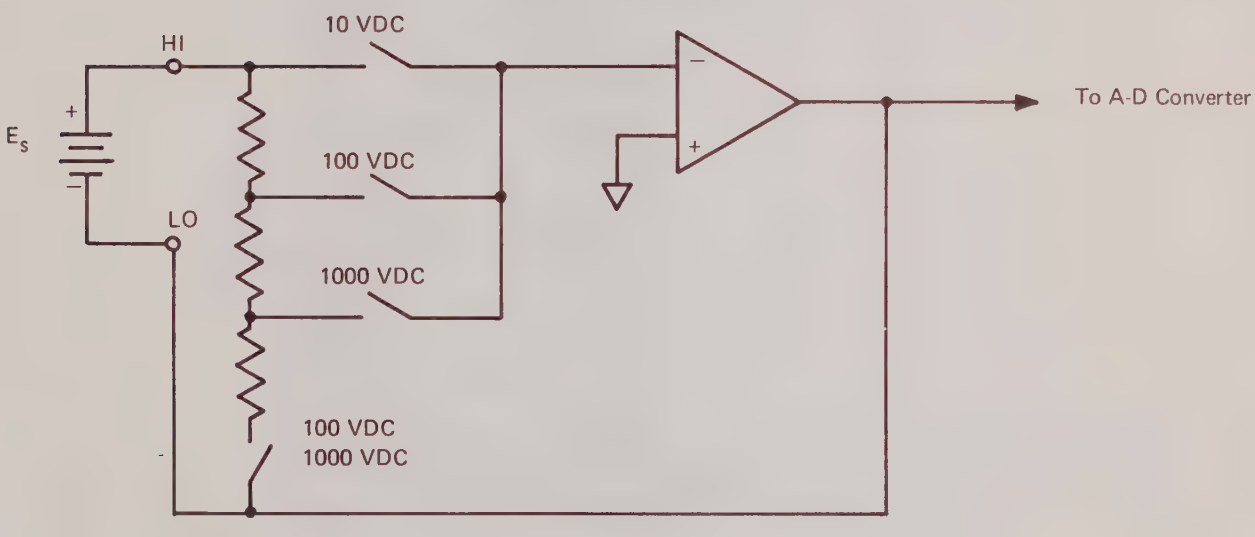


Figure 17. BUFFER WITH ATTENUATOR

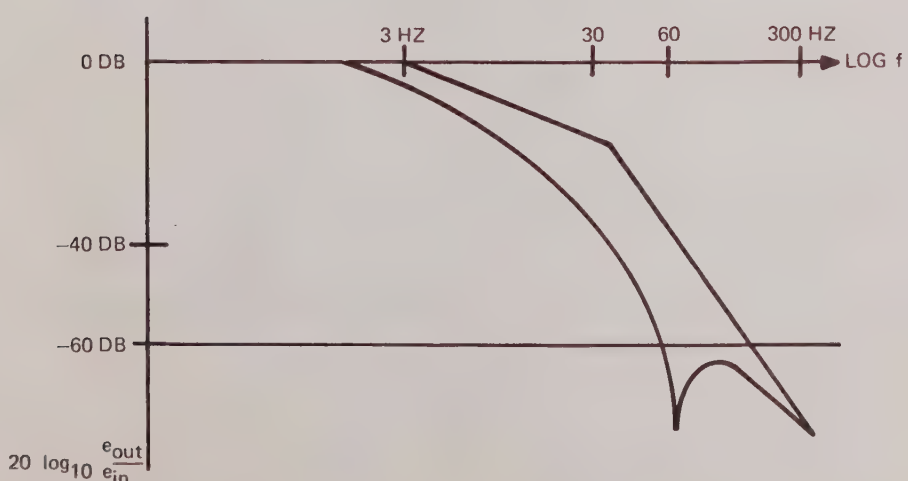
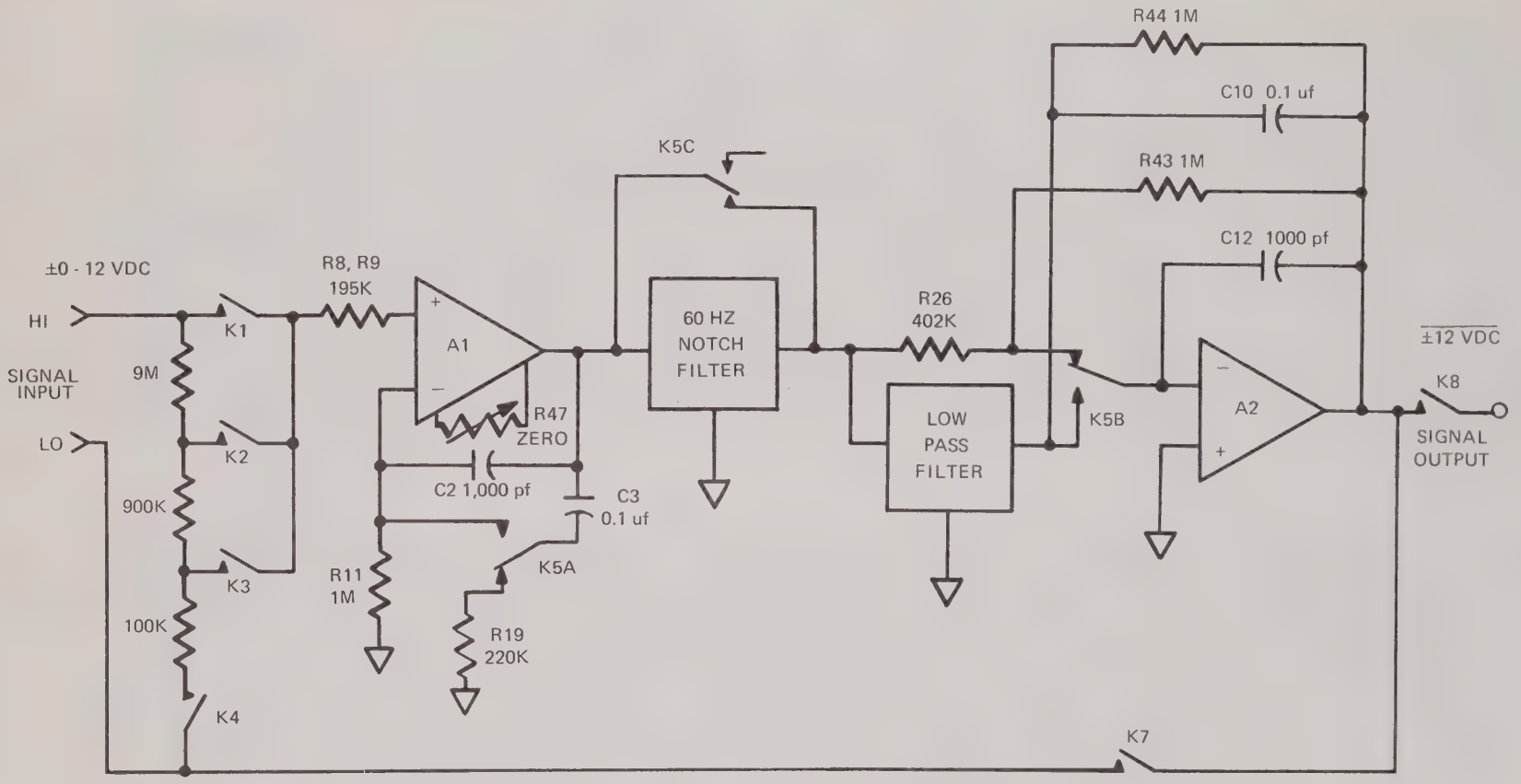


Figure 18. FILTER TRANSFER FUNCTION



RELAY OPERATION

K1	All KΩ Ranges MΩ 10 VDC
K2	100 VDC
K3	1000 VDC
K4	AC 100 VDC 1000 VDC
K5	Filter and any KΩ, MΩ or DCV
K7	All KΩ, MΩ and DC
K8	All DC, MΩ, 1000 KΩ and 100 KΩ

Figure 19. BLOCK DIAGRAM OF BUFFER

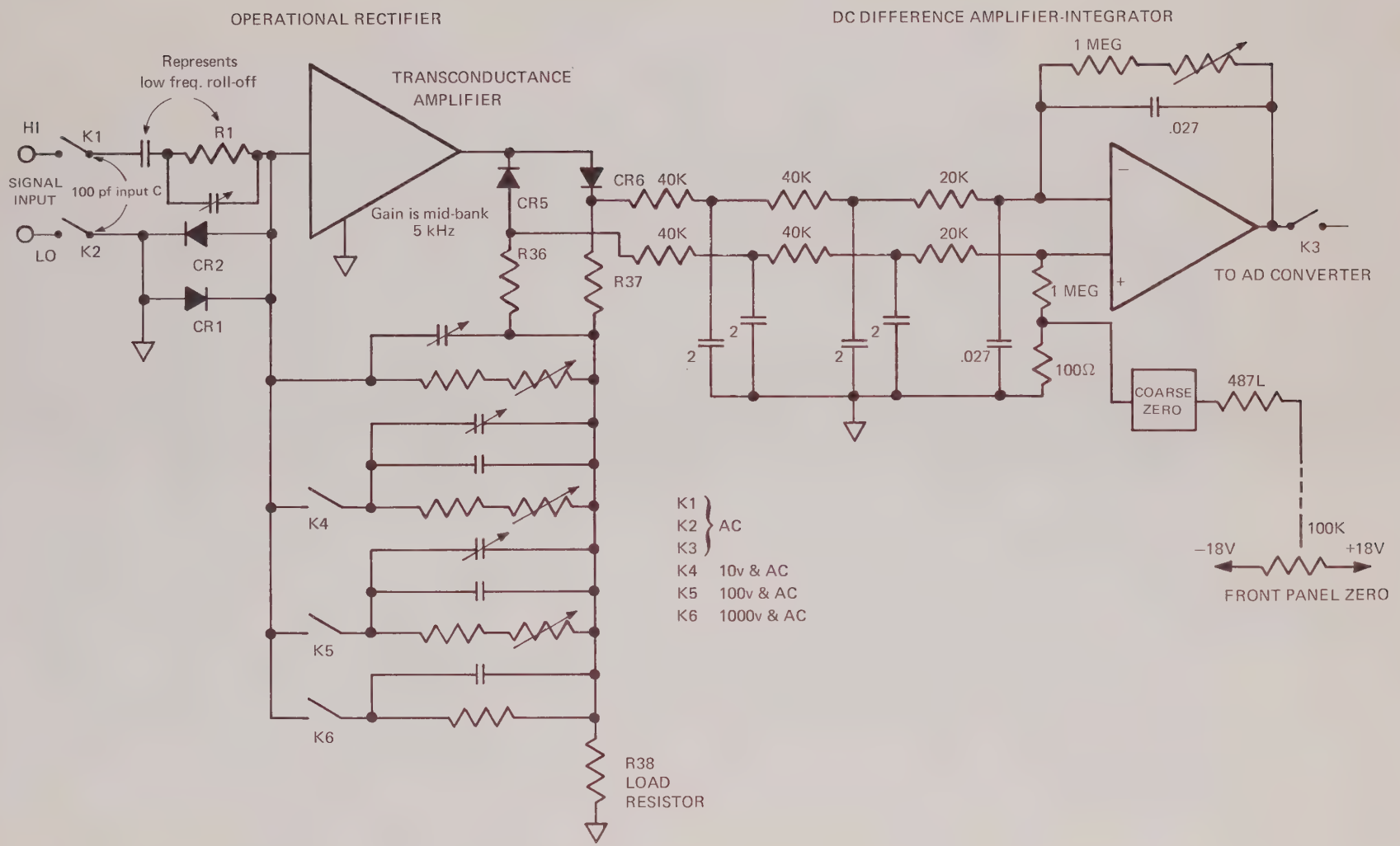


Figure 20. BLOCK DIAGRAM AC CONVERTER

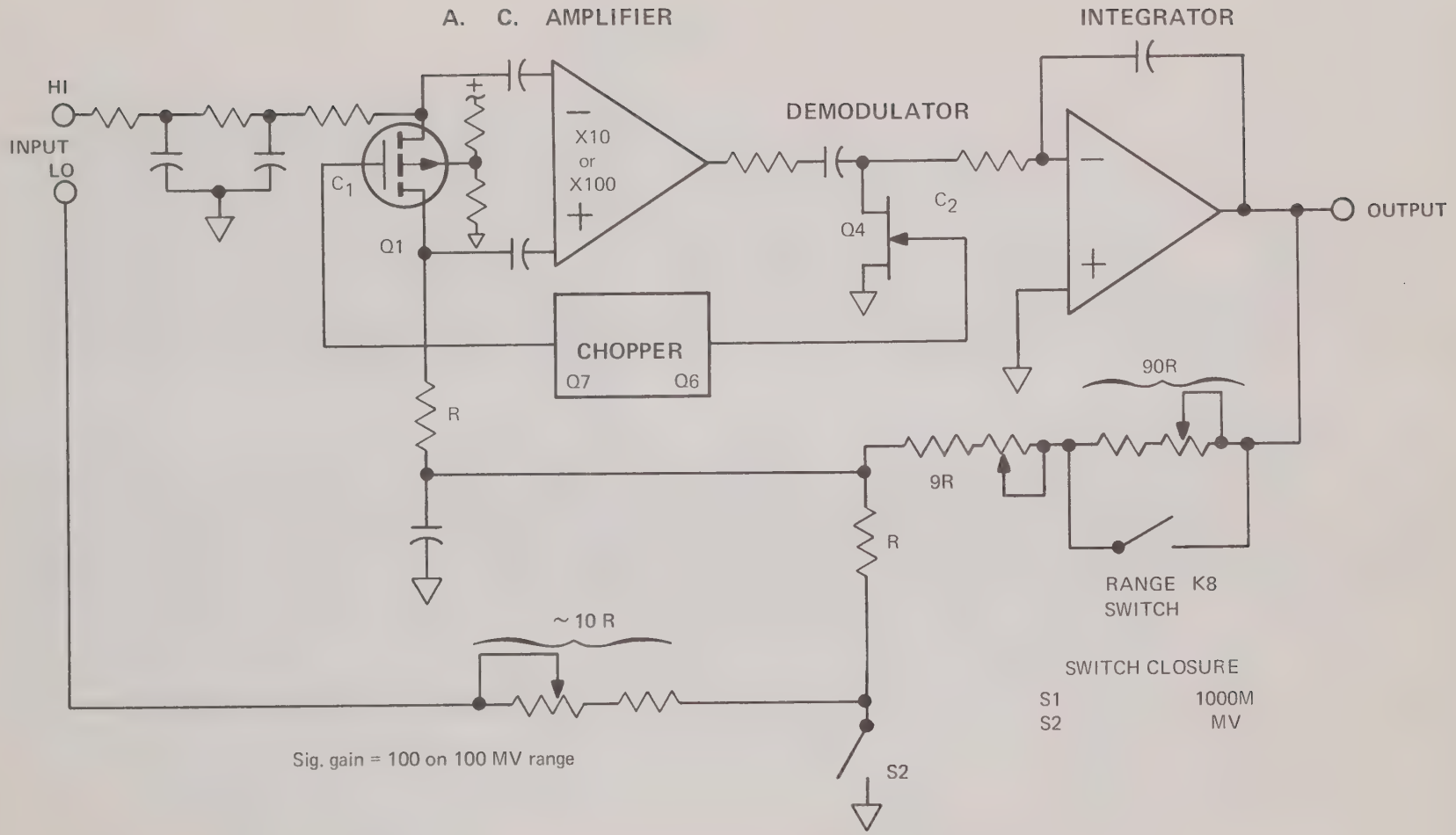
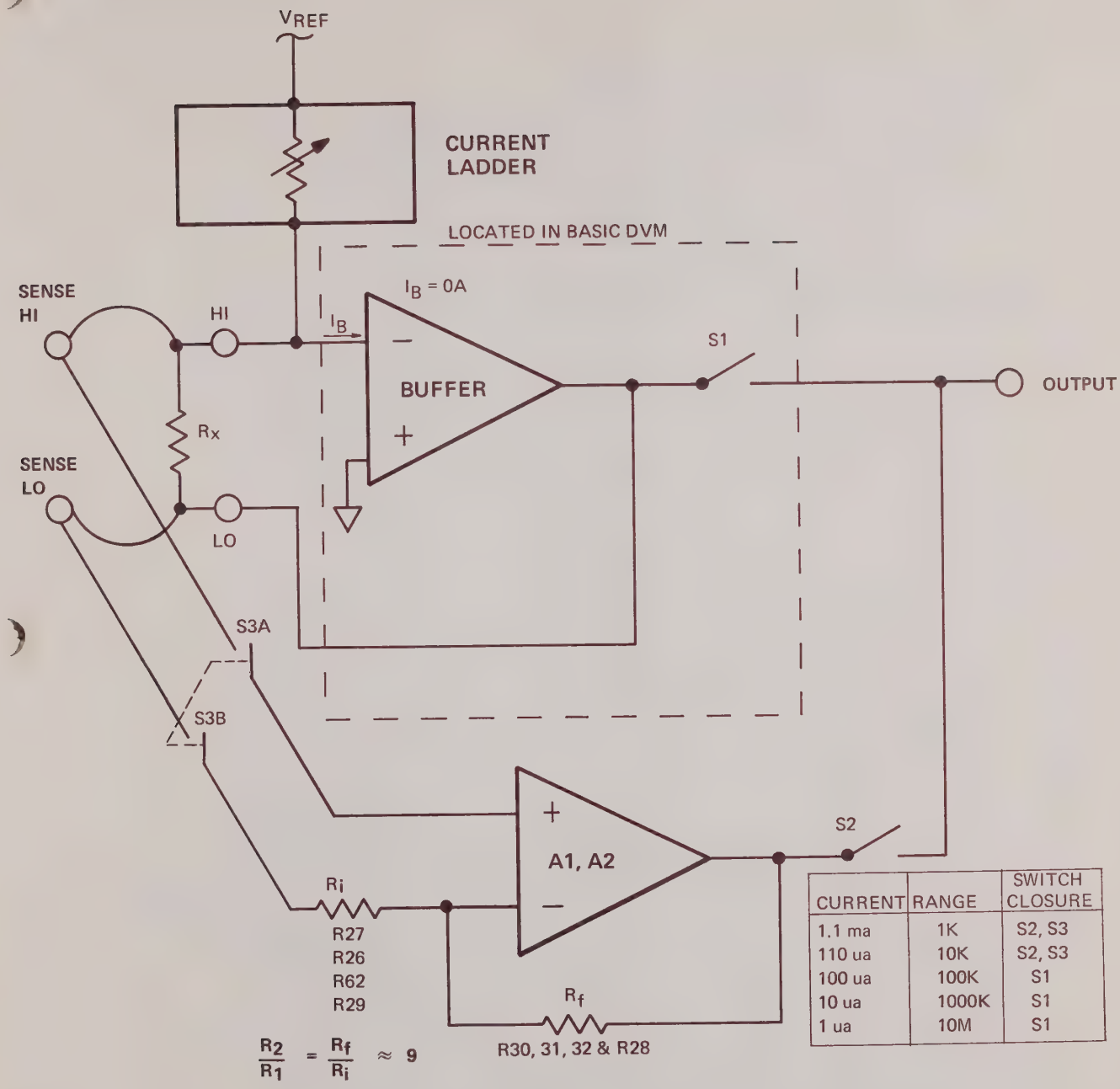


Figure 21. BLOCK DIAGRAM OF MILLIVOLT CONVERTER



CURRENT	RANGE	SWITCH CLOSURE
1.1 ma	1K	S2, S3
110 ua	10K	S2, S3
100 ua	100K	S1
10 ua	1000K	S1
1 ua	10M	S1

Figure 22. BLOCK DIAGRAM OF OHM CONVERTER

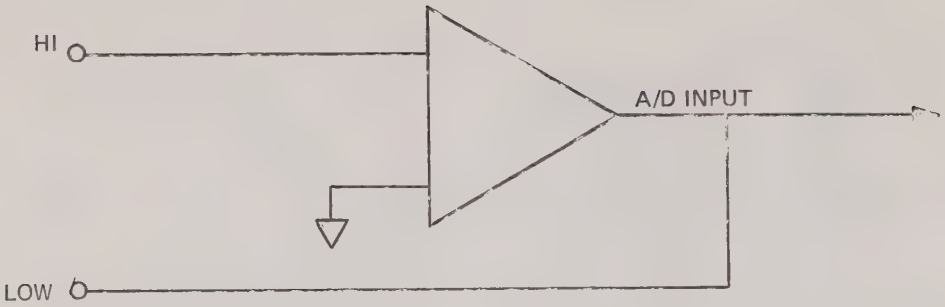


Figure 23.

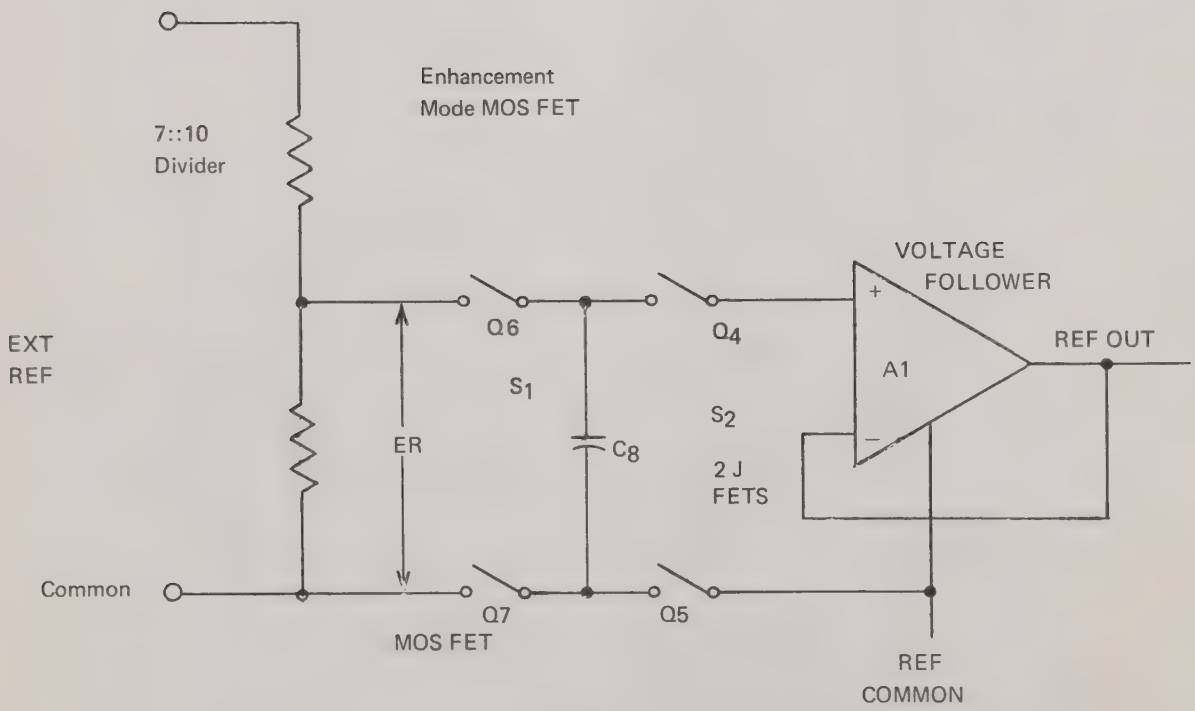


Figure 24.

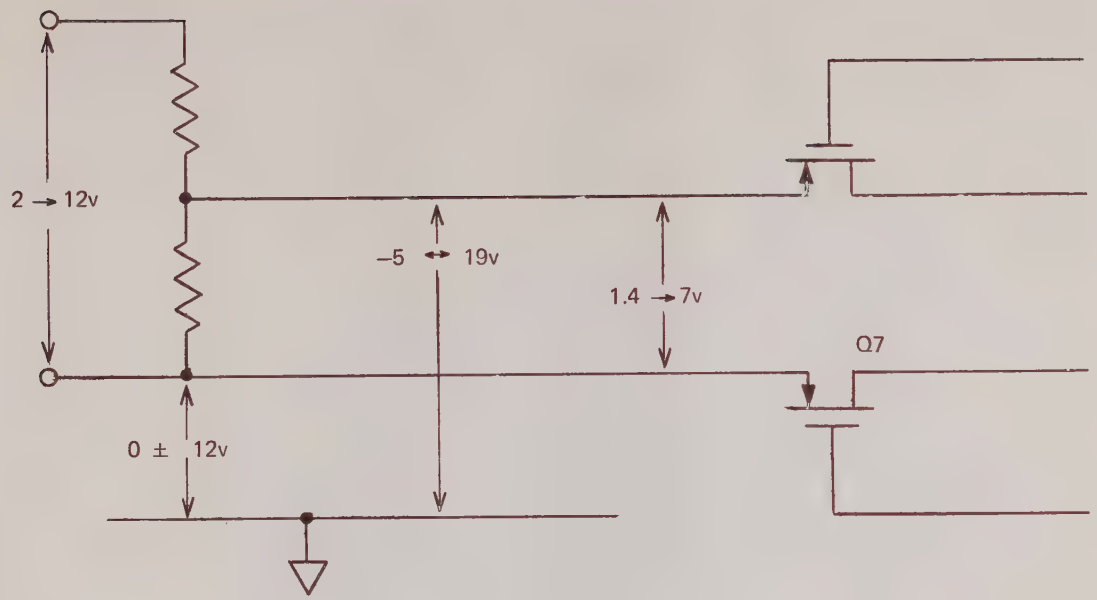


Figure 25

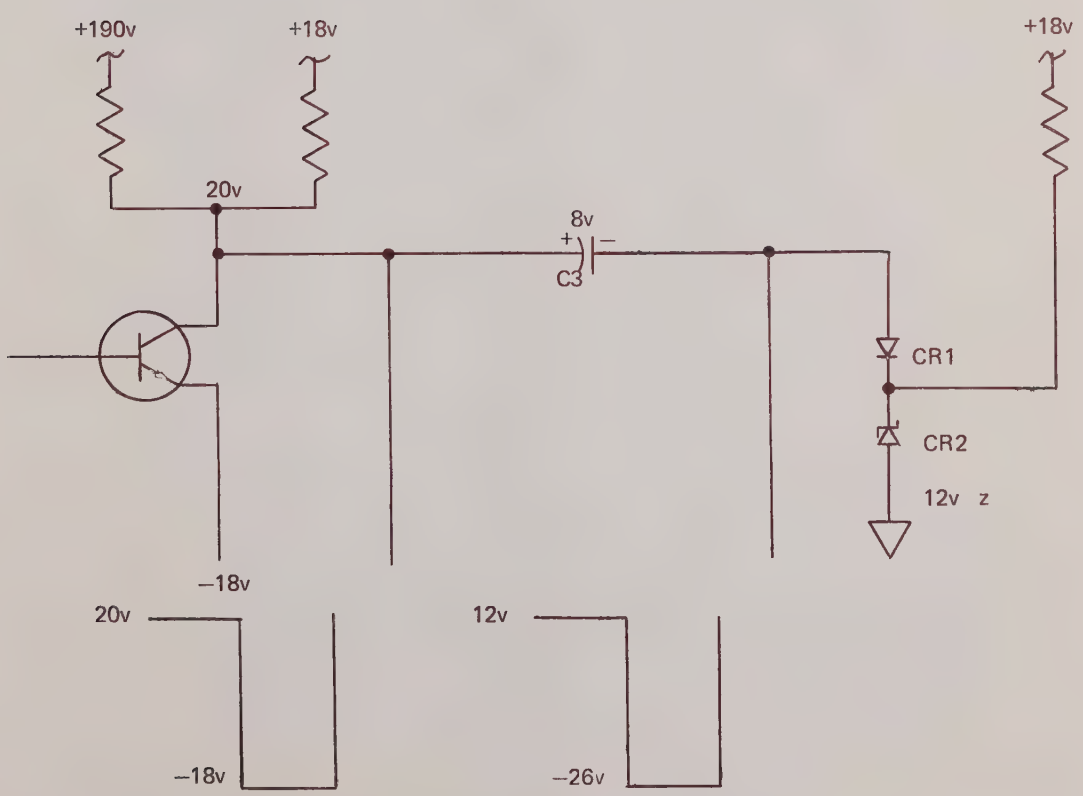


Figure 26

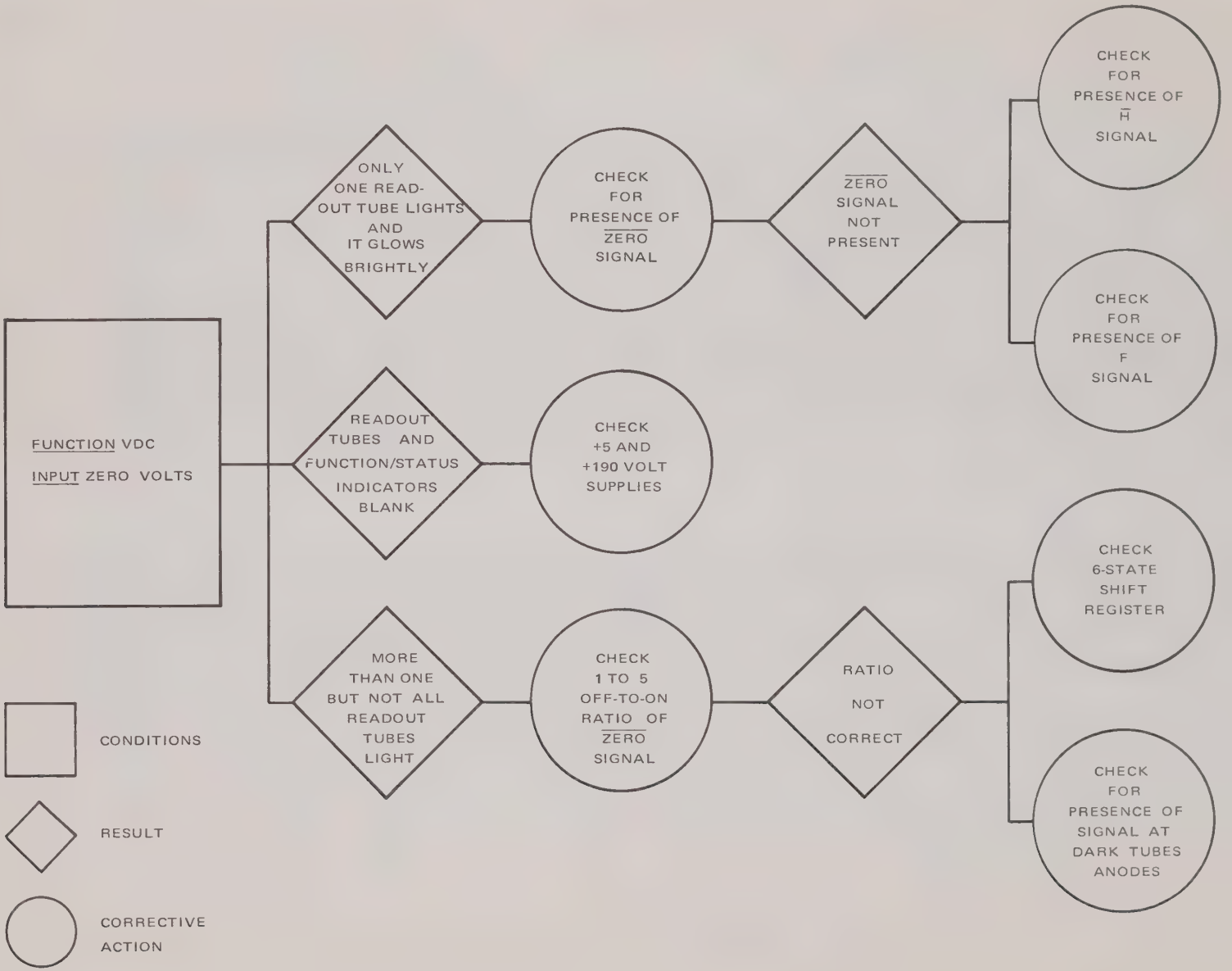

FUNCTION VDC
INPUT ZERO VOLTS
ONLY ONE READ-OUT TUBE LIGHTS AND IT GLOWS BRIGHTLY
CHECK FOR PRESENCE OF $\overline{\text{ZERO}}$ SIGNAL
$\overline{\text{ZERO}}$ SIGNAL NOT PRESENT
CHECK FOR PRESENCE OF $\overline{\text{H}}$ SIGNAL
CHECK FOR PRESENCE OF F SIGNAL
READOUT TUBES AND FUNCTION/STATUS INDICATORS BLANK
CHECK +5 AND +190 VOLT SUPPLIES
MORE THAN ONE BUT NOT ALL READOUT TUBES LIGHT
CHECK 1 TO 5 OFF-TO-ON RATIO OF $\overline{\text{ZERO}}$ SIGNAL
RATIO NOT CORRECT
CHECK 6-STATE SHIFT REGISTER
CHECK FOR PRESENCE OF SIGNAL AT DARK TUBES ANODES
CONDITIONS
RESULT
CORRECTIVE ACTION

Figure 27.

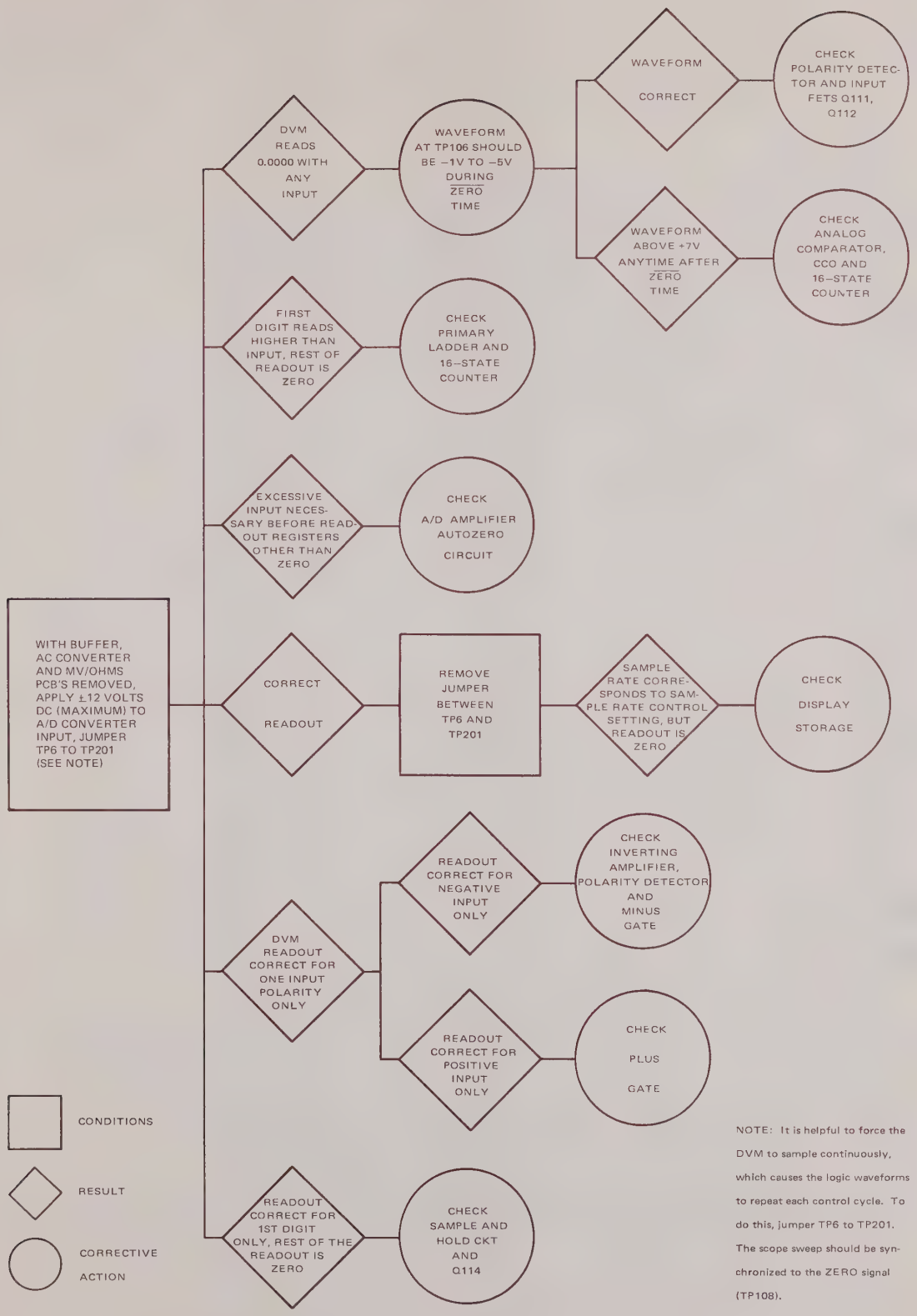
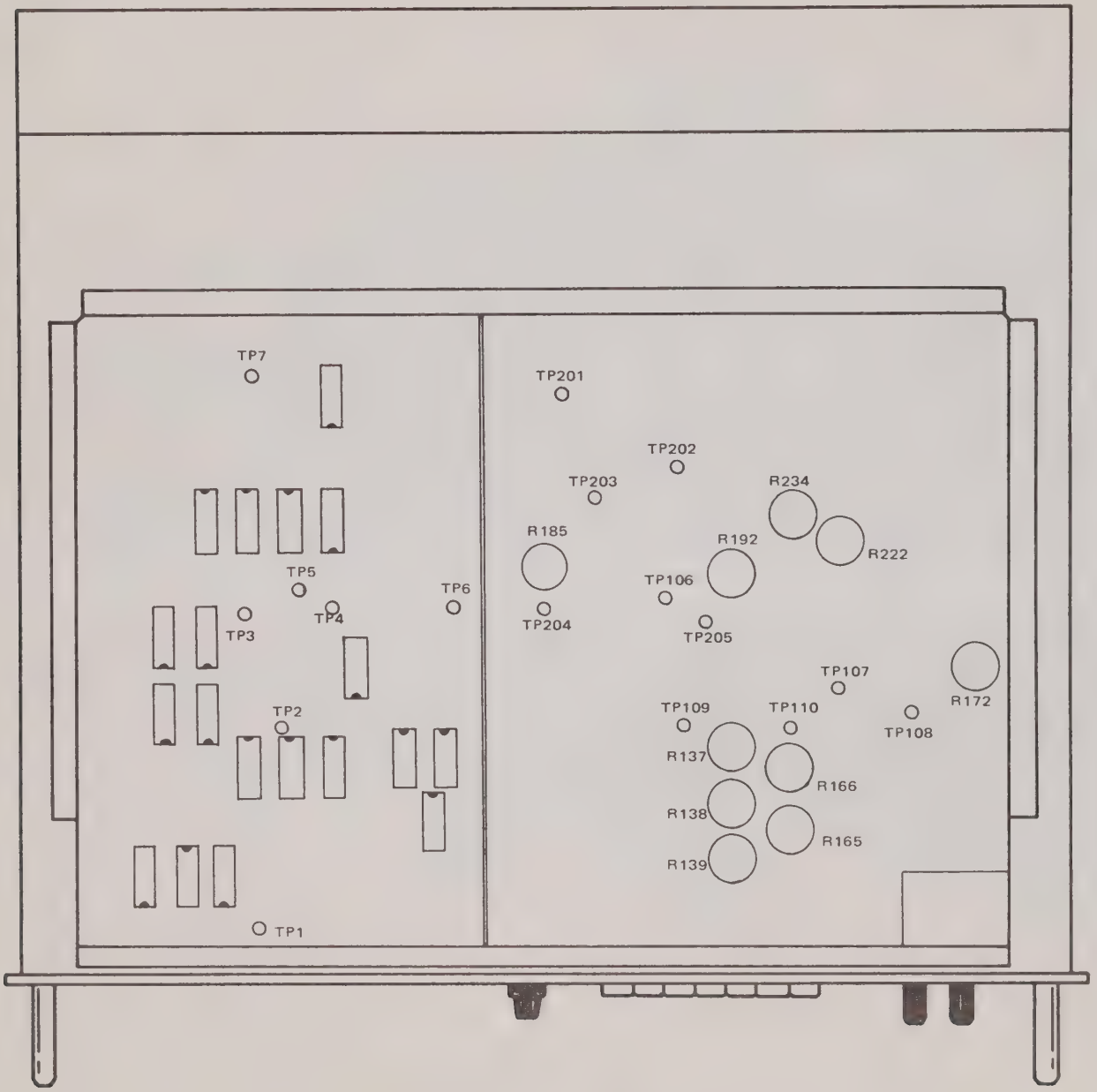

WITH BUFFER, AC CONVERTER AND MV/OHMS PCB'S REMOVED, APPLY ±12 VOLTS DC (MAXIMUM) TO A/D CONVERTER INPUT, JUMPER TP6 TO TP201 (SEE NOTE)
DVM READS 0.0000 WITH ANY INPUT
WAVEFORM AT TP106 SHOULD BE −1V TO −5V DURING ZERO TIME
WAVEFORM CORRECT
CHECK POLARITY DETECTOR AND INPUT FETS Q111, Q112
WAVEFORM ABOVE +7V ANYTIME AFTER ZERO TIME
CHECK ANALOG COMPARATOR, CCO AND 16−STATE COUNTER
FIRST DIGIT READS HIGHER THAN INPUT, REST OF READOUT IS ZERO
CHECK PRIMARY LADDER AND 16−STATE COUNTER
EXCESSIVE INPUT NECESSARY BEFORE READOUT REGISTERS OTHER THAN ZERO
CHECK A/D AMPLIFIER AUTOZERO CIRCUIT
CORRECT READOUT
REMOVE JUMPER BETWEEN TP6 AND TP201
SAMPLE RATE CORRESPONDS TO SAMPLE RATE CONTROL SETTING, BUT READOUT IS ZERO
CHECK DISPLAY STORAGE
DVM READOUT CORRECT FOR ONE INPUT POLARITY ONLY
READOUT CORRECT FOR NEGATIVE INPUT ONLY
CHECK INVERTING AMPLIFIER, POLARITY DETECTOR AND MINUS GATE
READOUT CORRECT FOR POSITIVE INPUT ONLY
CHECK PLUS GATE
READOUT CORRECT FOR 1ST DIGIT ONLY, REST OF THE READOUT IS ZERO
CHECK SAMPLE AND HOLD CKT AND Q114
CONDITIONS
RESULT
CORRECTIVE ACTION
NOTE: It is helpful to force the DVM to sample continuously, which causes the logic waveforms to repeat each control cycle. To do this, jumper TP6 to TP201. The scope sweep should be synchronized to the ZERO signal (TP108).

Figure 28. TROUBLESHOOTING DVM ANALOG CIRCUITRY



TP 1	+190 Anode Strobe
TP 2	H (Clock)
TP 3	Ground
TP 4	$\overline{\text{ZERO}}$
TP 5	F
TP 6	Trigger Input
TP 7	Range Pulsing
TP 106	A/D Amp. Out
TP 107	VCO
TP 108	$\overline{\text{ZERO}}$
TP 109	Ground
TP 110	Pri. Ladder Out
TP 111	Inv. Amp. Out
TP 201	+5v
TP 202	+190v
TP 203	−18v
TP 204	+18v
TP 205	+7v
R 137	Ladder Cal 4
R 138	Ladder Cal 2
R 139	Ladder Cal 1
R 165	− Cal
R 166	+ Cal
R 172	Comparator Level
R 185	Remainder Cal
R 192	A-D Zero
R 222	+7v Ref.
R 234	+18v

Figure 29.

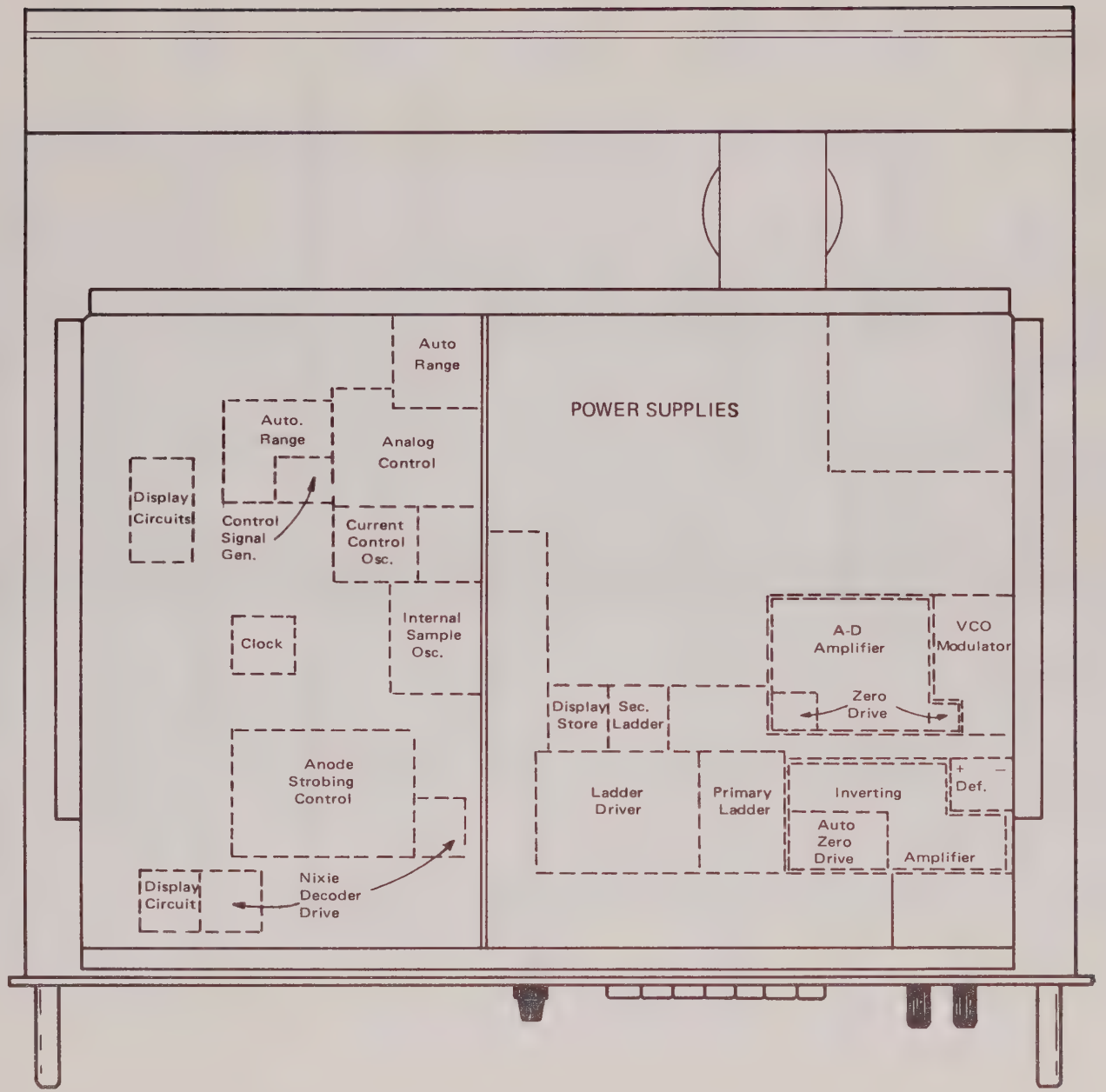
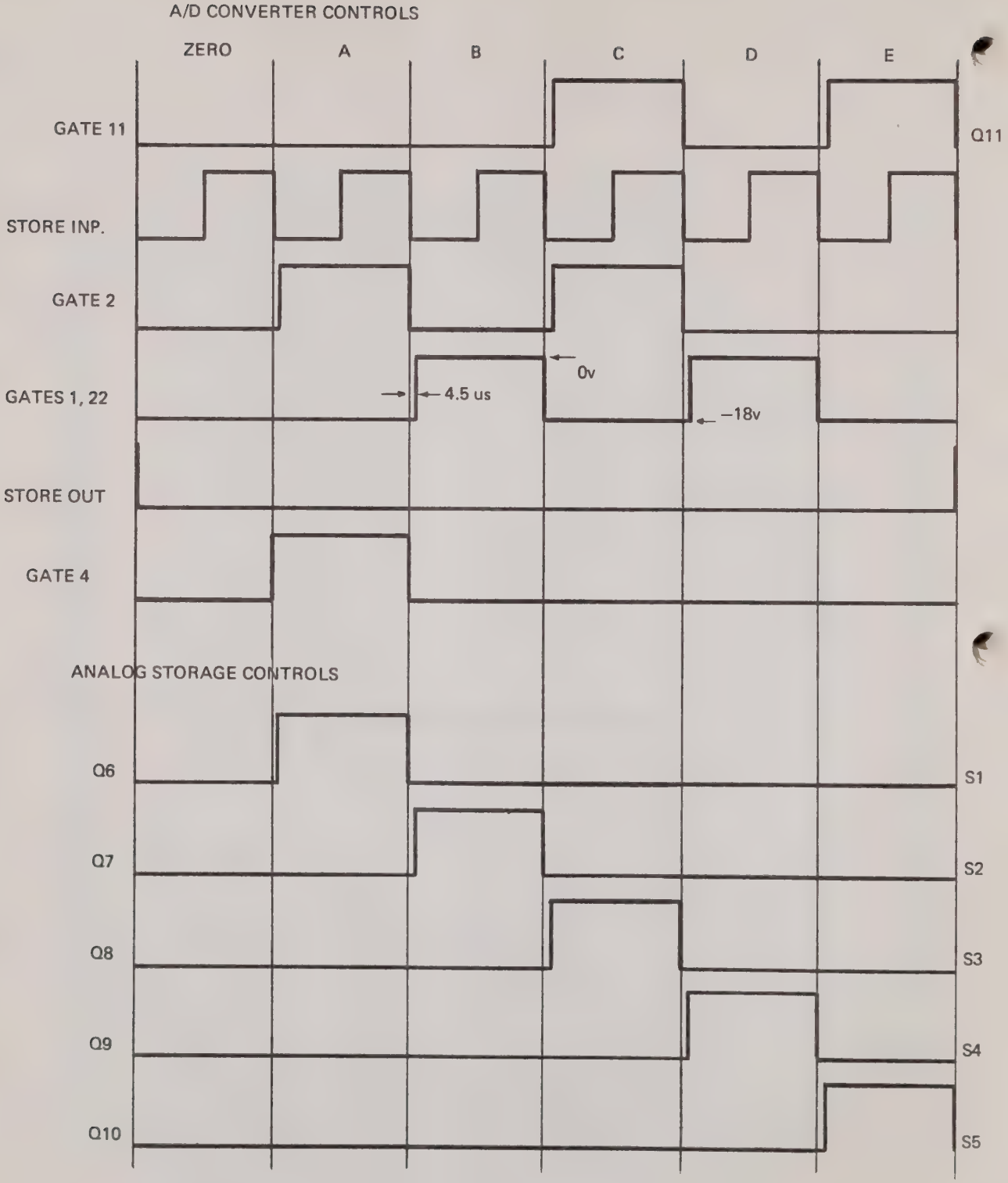

Auto
Range
POWER SUPPLIES
Auto.
Range
Analog
Control
Display
Circuits
Control
Signal
Gen.
Current
Control
Osc.
Internal
Sample
Osc.
Clock
A-D
Amplifier
VCO
Modulator
Zero
Drive
Display
Store
Sec.
Ladder
Anode
Strobing
Control
Ladder
Driver
Primary
Ladder
Inverting
Def.
Auto
Zero
Drive
Amplifier
Display
Circuit
Nixie
Decoder
Drive

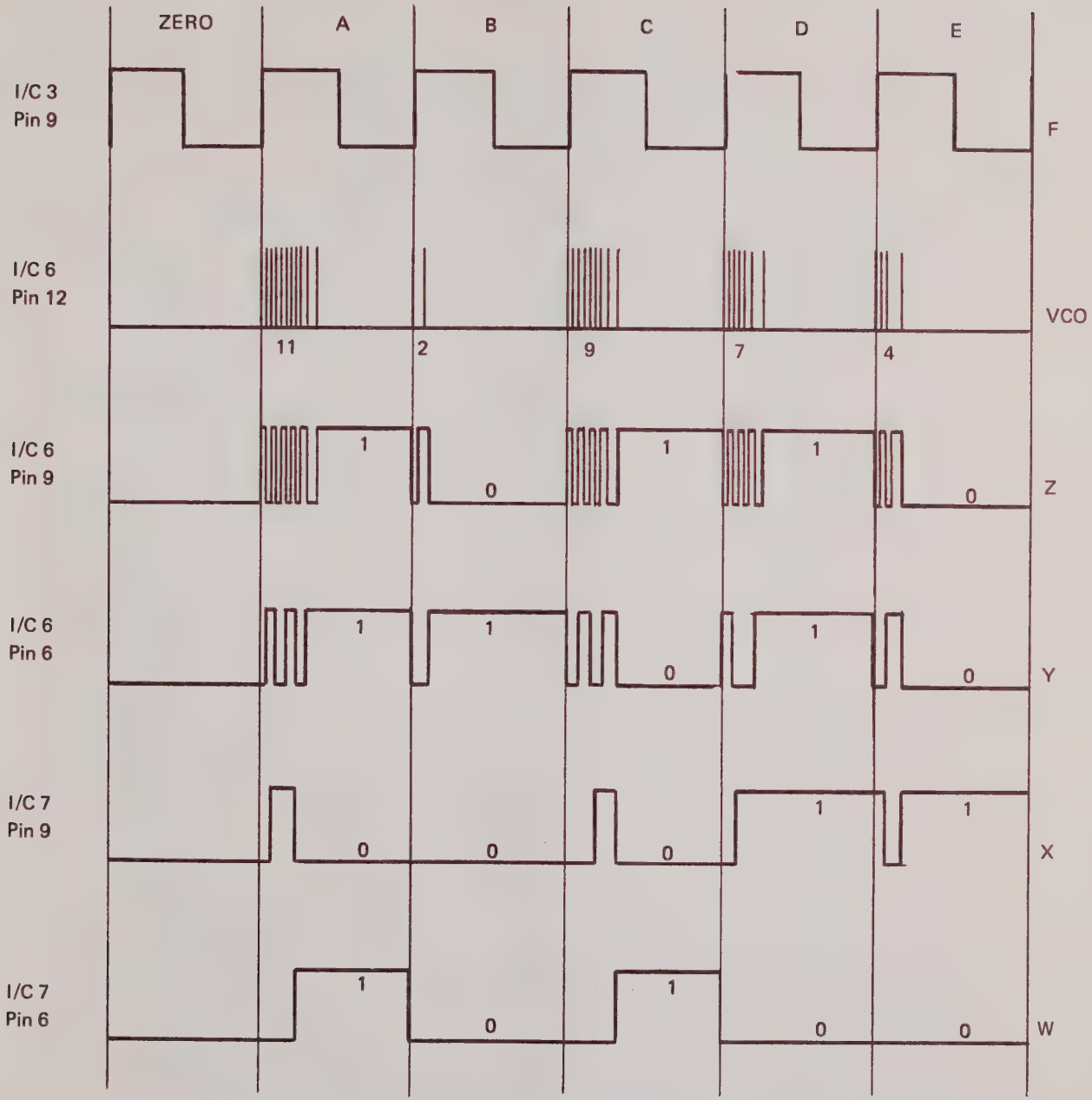
Figure 30.



NOTE: Logic 1 = 0 VDC
Logic 0 = −18 VDC

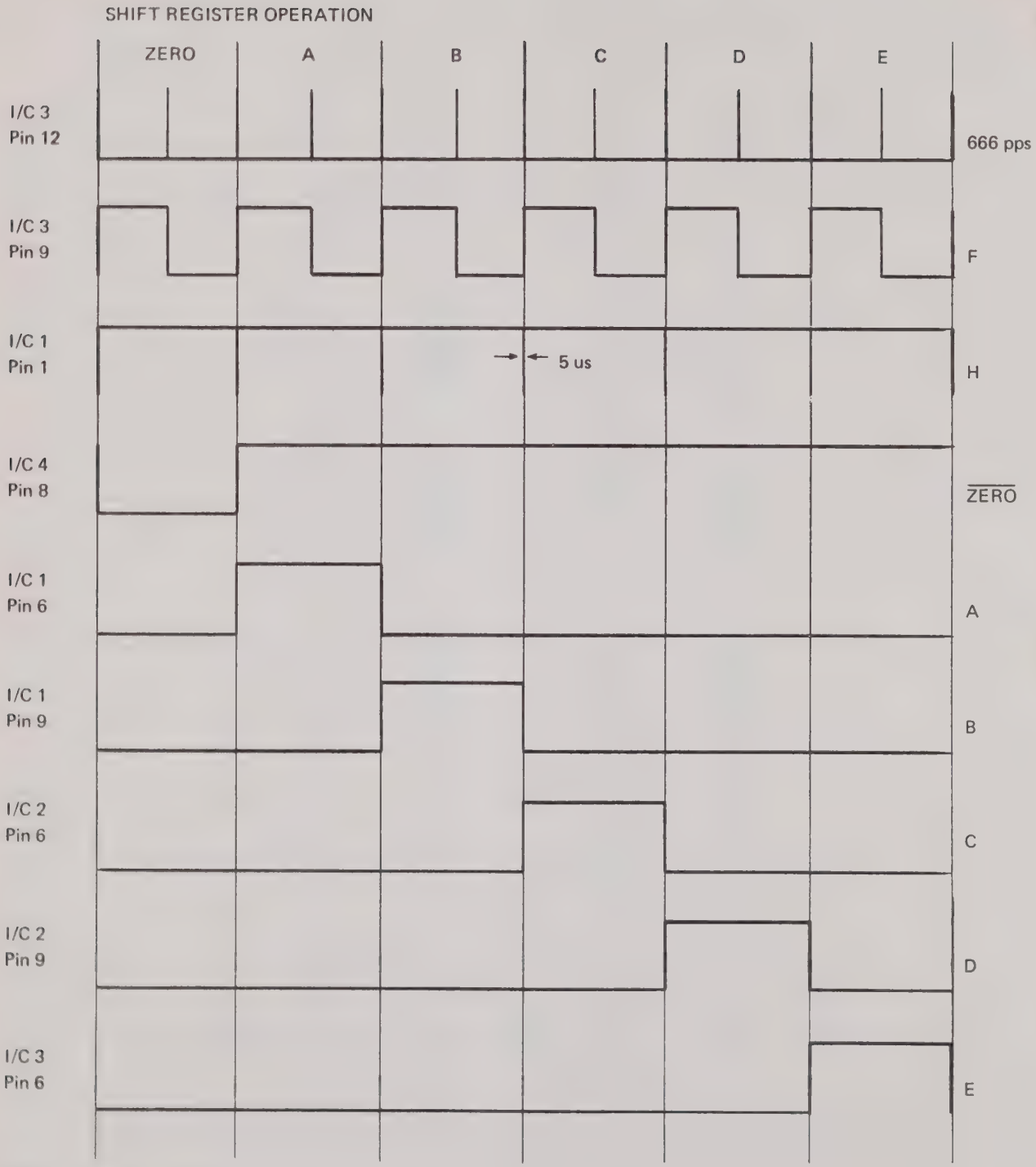
Figure 31.

16 STATE BINARY COUNTER OPERATION



NOTE: Example display is 11.2974v
Logic 0 = < 0.5v
Logic 1 = > 3.5v

Figure 32.



NOTE: Logic 0 = < 0.5v
Logic 1 = > 3.5v

Figure 33.

LOGIC FUNCTIONS (Basic Instrument)

IC 12 Pin 14	$1\ \overline{VDC}\ \overline{M\Omega}\ \overline{MV}$
IC 10 Pin 14	$10\ \overline{MV}$
IC 10 Pin 3	$100\ \overline{M\Omega}$
IC 10 Pin 13	$1000\ \overline{M\Omega}$
IC 11 Pin 2	$\overline{1\ \overline{VDC}\ \overline{Mv} + M\Omega + 10\ \overline{MV}}$
IC 11 Pin 14	$\overline{100\ \overline{M\Omega} + MV + 1000\ \overline{M\Omega}}$
IC 12 Pin 2	$\overline{10\ \overline{MV} + M\Omega + 1000 + DC\overline{ab}}$
IC 10 Pin 2	$\overline{100\ \overline{M\Omega} + 1\ \overline{VDC}\ \overline{M\Omega}\ \overline{MV}}$
IC 4 Pin 6	$\overline{ab} + \overline{a}VDC + \overline{b}MV + 100 + 10\ \overline{MV} + M\Omega + \overline{\overline{W}\overline{X}\overline{Y}\overline{Z}} + 1000$
IC15 Pin 11	$\overline{\overline{ab} + \overline{a}VDC + \overline{b}MV}$
IC 15 Pin 6	$\overline{a} + MV$
IC 15 Pin 3	$\overline{b} + VDC$
IC 15 Pin 8	$\overline{WX}$
IC 13 Pin 13	$WX\overline{b}$
IC 13 Pin 14	$\overline{ab}\ \overline{\overline{a}VDC}\ \overline{\overline{b}MV}\ \overline{100}\ \overline{1000}\ \overline{10\ \overline{MV}}\ \overline{M\Omega}\ \overline{\overline{W}\overline{X}\overline{Y}\overline{Z}}$
IC 19 Pin 6	(UP + DN) A
IC 19 Pin 8	$\overline{UP}\ \overline{DN} + \overline{A} + F + \overline{M}$
IC 8 Pin 2	$WYZ\ (1\ \overline{VDC}\ \overline{MV} + 10\ \overline{MV} + 100 + M\Omega + ab)$
IC 8 Pin 14	$\overline{1\ \overline{VDC}\ \overline{MV} + 10\ \overline{MV} + 100 + M\Omega + ab}$
IC 9 Pin 13	$WZ\overline{A}$
IC 9 Pin 14	$\overline{F}EM$
IC 16 Pin 3	ab
IC 11 Pin 13	$VDC\ \overline{ab}$
IC 17 Pin 16	$\overline{\overline{W}\overline{X}\overline{Y}\overline{Z} + W\overline{X}Y\overline{Z}}$
IC 17 Pin 15	$\overline{\overline{W}\overline{X}\overline{Y}Z + W\overline{X}YZ}$
IC 17 Pin 8	$\overline{\overline{W}\overline{X}Y\overline{Z} + WX\overline{Y}\overline{Z}}$
IC 17 Pin 9	$\overline{\overline{W}\overline{X}YZ + WX\overline{Y}Z}$
IC 17 Pin 13	$\overline{\overline{W}X\overline{Y}\overline{Z} + WXY\overline{Z}}$
IC 17 Pin 14	$\overline{\overline{W}X\overline{Y}Z + WXYZ}$
IC 17 Pin 11	$\overline{\overline{W}XY\overline{Z}}$
IC 17 Pin 12	$\overline{\overline{W}XYZ}$
IC 17 Pin 1	$\overline{W\overline{X}\overline{Y}\overline{Z}}$
IC 17 Pin 2	$\overline{W\overline{X}\overline{Y}Z}$
Q11 Collector	$M\overline{H}$ (C+E)
Q12 Collector	F
Q13 Collector	$M\overline{H}$ (A+C)
Q14 Collector	$M\overline{H}$ (B+D)
Q15 Collector	$\overline{M}$
Q16 Collector	MA
Q36 Collector	$\overline{F}E$
Q37 Collector	$\overline{F}D$
Q38 Collector	$\overline{F}C$

Figure 34. LOGIC FUNCTIONS (Sheet 1 of 2)

LOGIC FUNCTIONS (Continued)

Q39 Collector	$\bar{F}B$
Q40 Collector	$\bar{F}A$
Q41 Collector	$\overline{WY}$
Q21 Collector	$\bar{a}\bar{b}$
Q22 Collector	$\bar{a}b$
Q23 Collector	$a\bar{b}$
Q24 Collector	ab
Q6 Collector	$A\bar{H}$
Q7 Collector	$B\bar{H}$
Q8 Collector	$C\bar{H}$
Q9 Collector	$D\bar{H}$
Q10 Collector	$E\bar{H}$
Q29 Emitter	a buffered
Q30 Emitter	b buffered

Figure 34. LOGIC FUNCTIONS (Sheet 2 of 2)

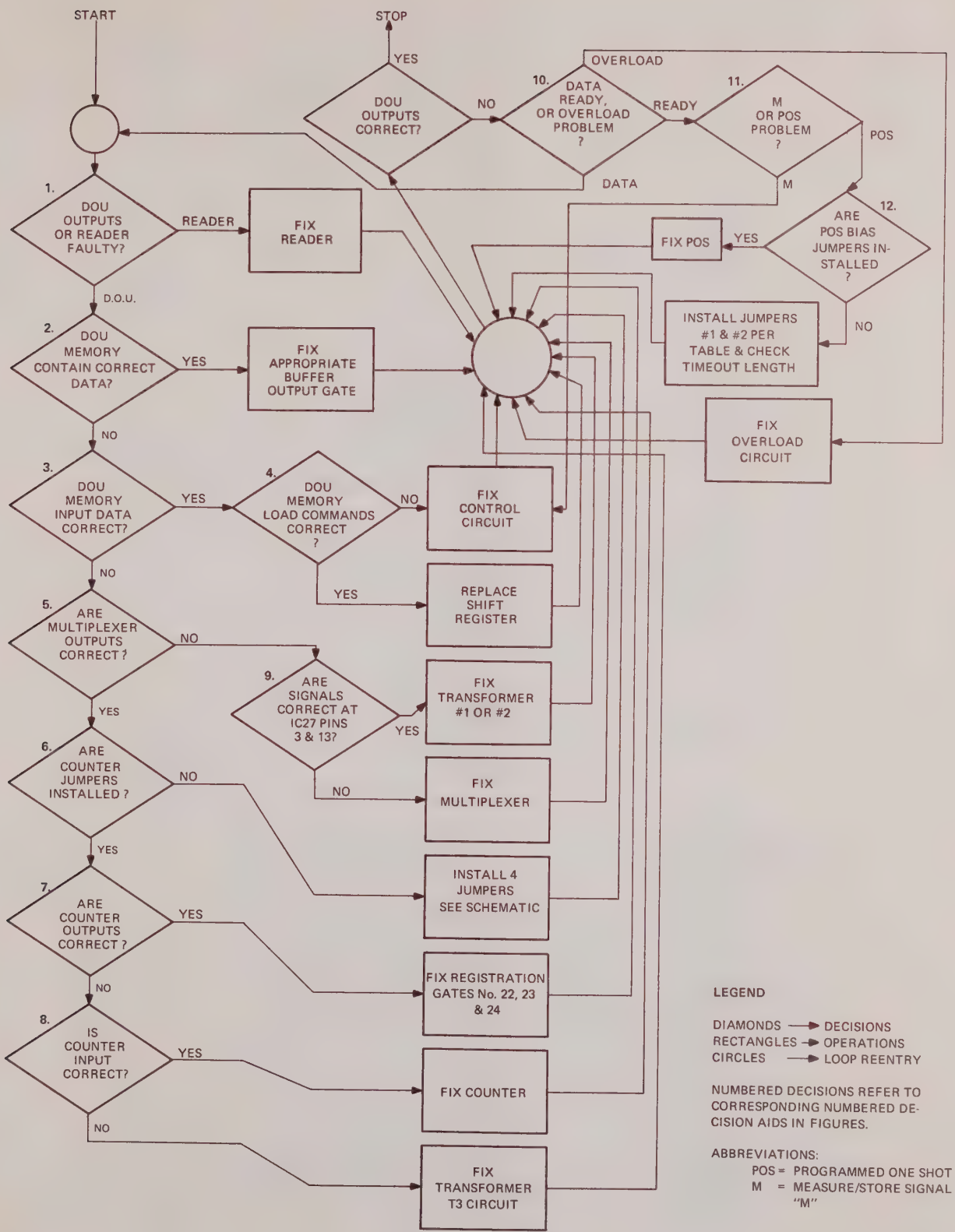


Figure 35. DECISION FLOW CHART –DOU TROUBLESHOOTING

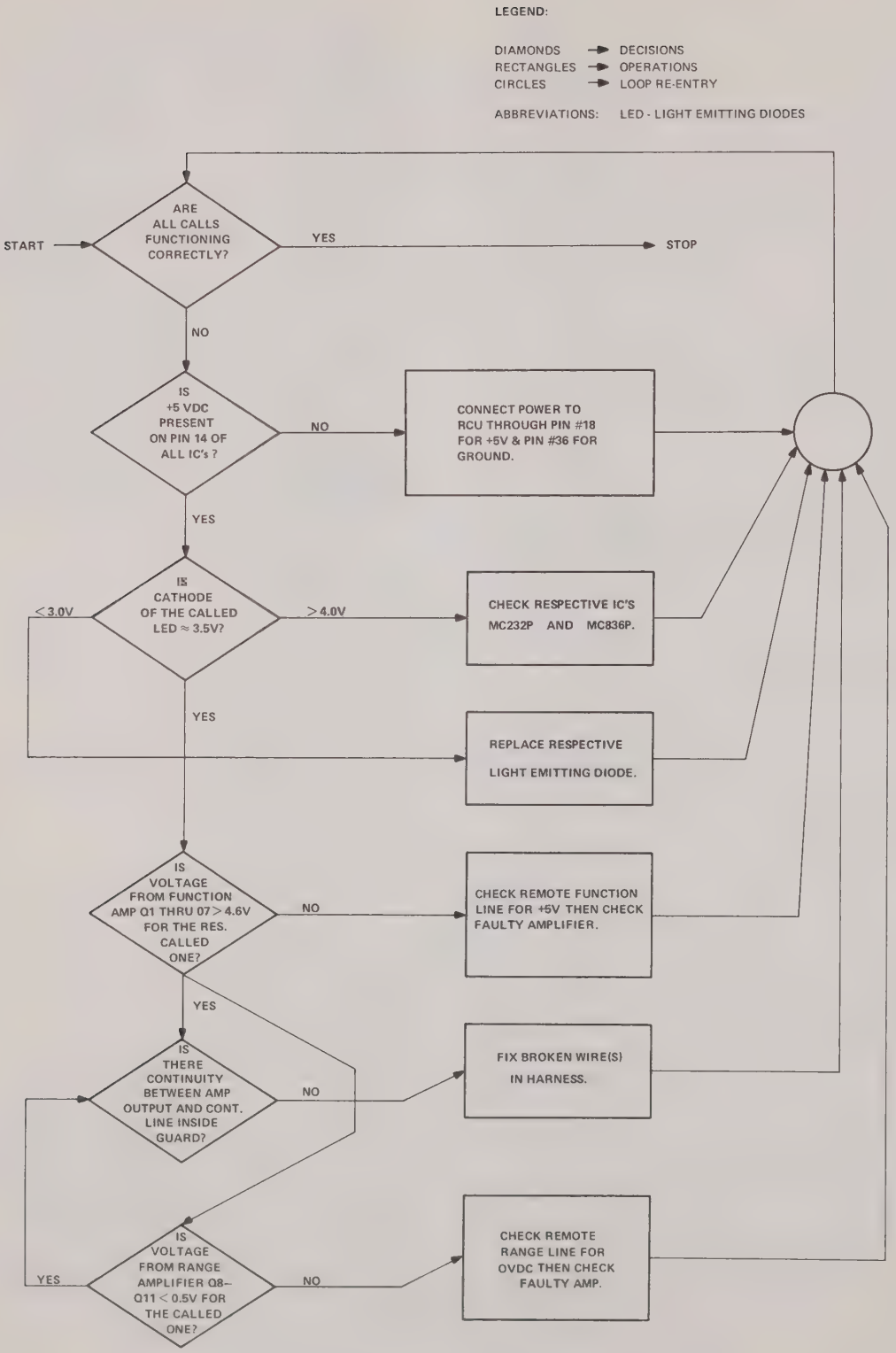

LEGEND:
DIAMONDS → DECISIONS
RECTANGLES → OPERATIONS
CIRCLES → LOOP RE-ENTRY
ABBREVIATIONS: LED - LIGHT EMITTING DIODES
START
ARE ALL CALLS FUNCTIONING CORRECTLY?
YES
STOP
NO
IS +5 VDC PRESENT ON PIN 14 OF ALL IC's ?
NO
CONNECT POWER TO RCU THROUGH PIN #18 FOR +5V & PIN #36 FOR GROUND.
YES
IS CATHODE OF THE CALLED LED ≈ 3.5V?
< 3.0V
> 4.0V
CHECK RESPECTIVE IC'S MC232P AND MC836P.
YES
REPLACE RESPECTIVE LIGHT EMITTING DIODE.
IS VOLTAGE FROM FUNCTION AMP Q1 THRU 07 > 4.6V FOR THE RES. CALLED ONE?
NO
CHECK REMOTE FUNCTION LINE FOR +5V THEN CHECK FAULTY AMPLIFIER.
YES
IS THERE CONTINUITY BETWEEN AMP OUTPUT AND CONT. LINE INSIDE GUARD?
NO
FIX BROKEN WIRE(S) IN HARNESS.
IS VOLTAGE FROM RANGE AMPLIFIER Q8–Q11 < 0.5V FOR THE CALLED ONE?
YES
NO
CHECK REMOTE RANGE LINE FOR OVDC THEN CHECK FAULTY AMP.

Figure 36.

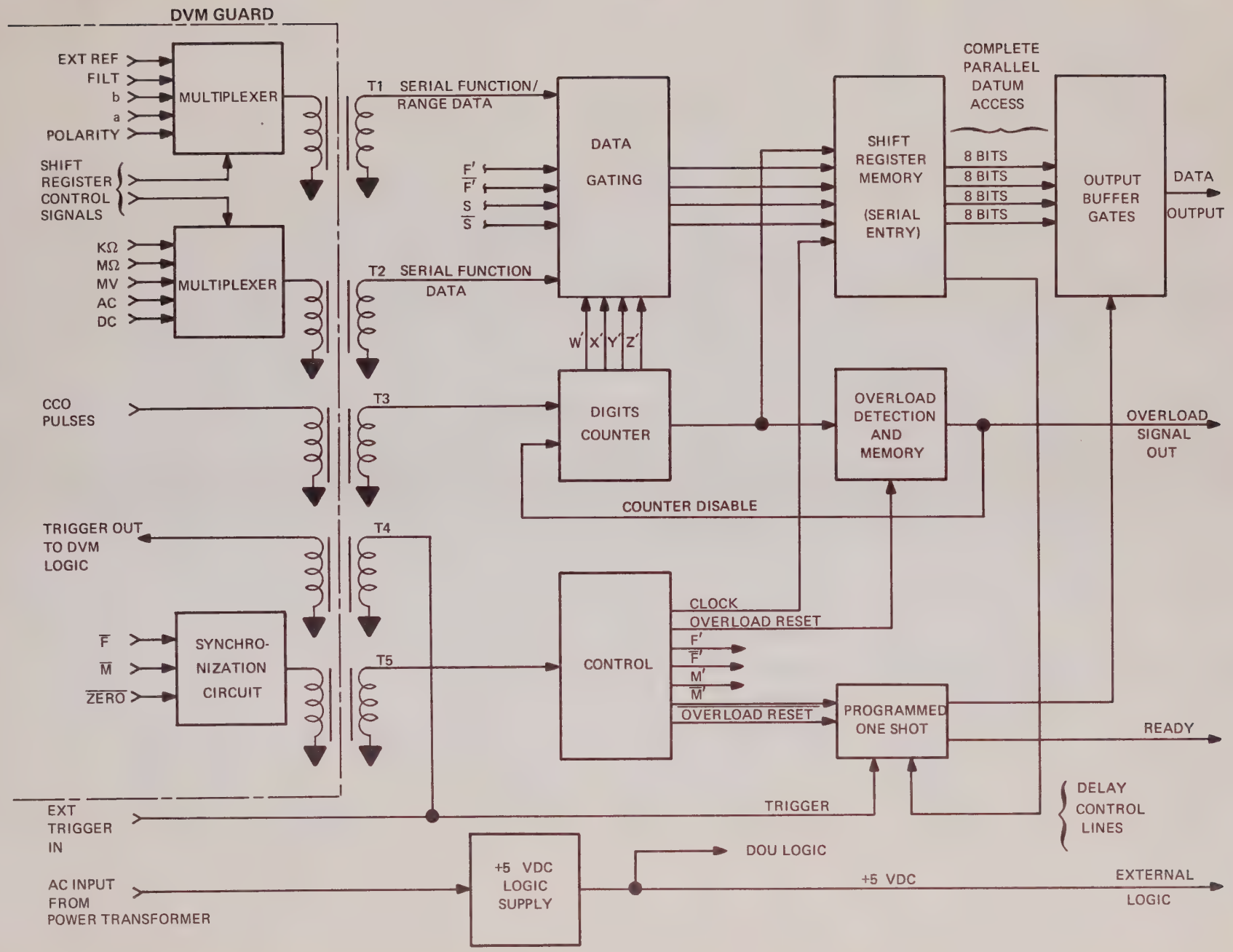


Figure 39. DATA OUTPUT UNIT BLOCK DIAGRAM

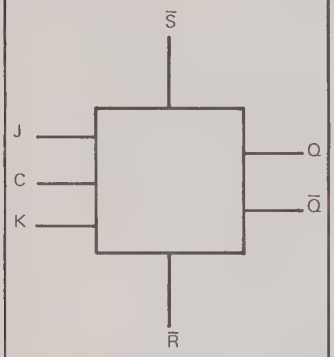
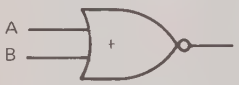
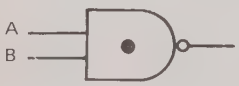
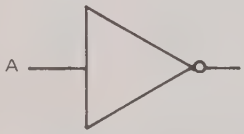
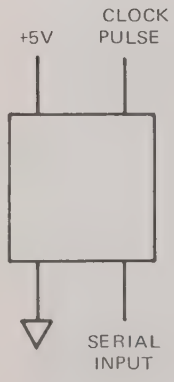
LOGIC SYMBOL	NAME	DESCRIPTION
	J-K Flip Flop	Operation of the J-K flip flop is shown by the following truth tables. Note that "S" and "R" inputs are dominant over "J" and "K" inputs. J K Q_{n+1}: 0 0 Q_n; 0 1 0; 1 0 1; 1 1 $\overline{Q}_n$ S R Q $\overline{Q}$: 0 0 Undefined; 0 1 1 0 Set; 1 0 0 1 Reset; 1 1 Normal Condition
	NOR Gate	The following table shows gate and inverter operation, Although only two-input gates are shown, operation is identical for gates having additional inputs. A B NOR NAND INVERTER 0 0 1 1 1 0 1 1 1 1 1 0 0 1 0 1 1 0 0 0
	NAND Gate	
	Inverter	
	Shift Register	Four 8-bit, serial-in parallel-out shift registers are used. A logical "1" at the input enters a logical "1" into the register. The register output terminals are not shown on the schematic; however, they are given in the following table: Shift Register Outputs Q1 3 Q2 4 Q3 5 Q4 6 Q5 10 Q6 11 Q7 12 Q8 13

Figure 40. EXPLANATION OF LOGIC SYMBOLOGY USED IN DOU

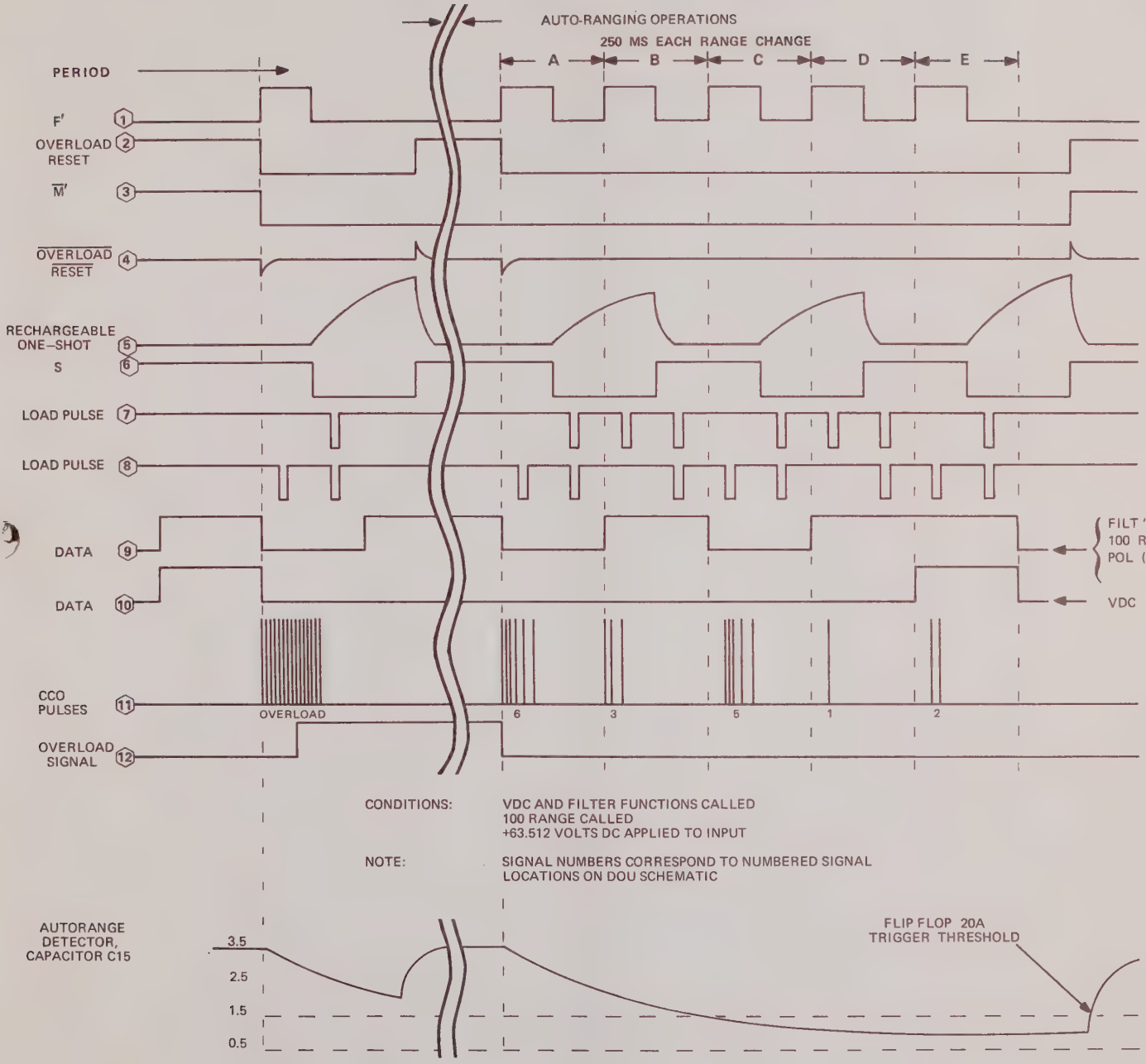
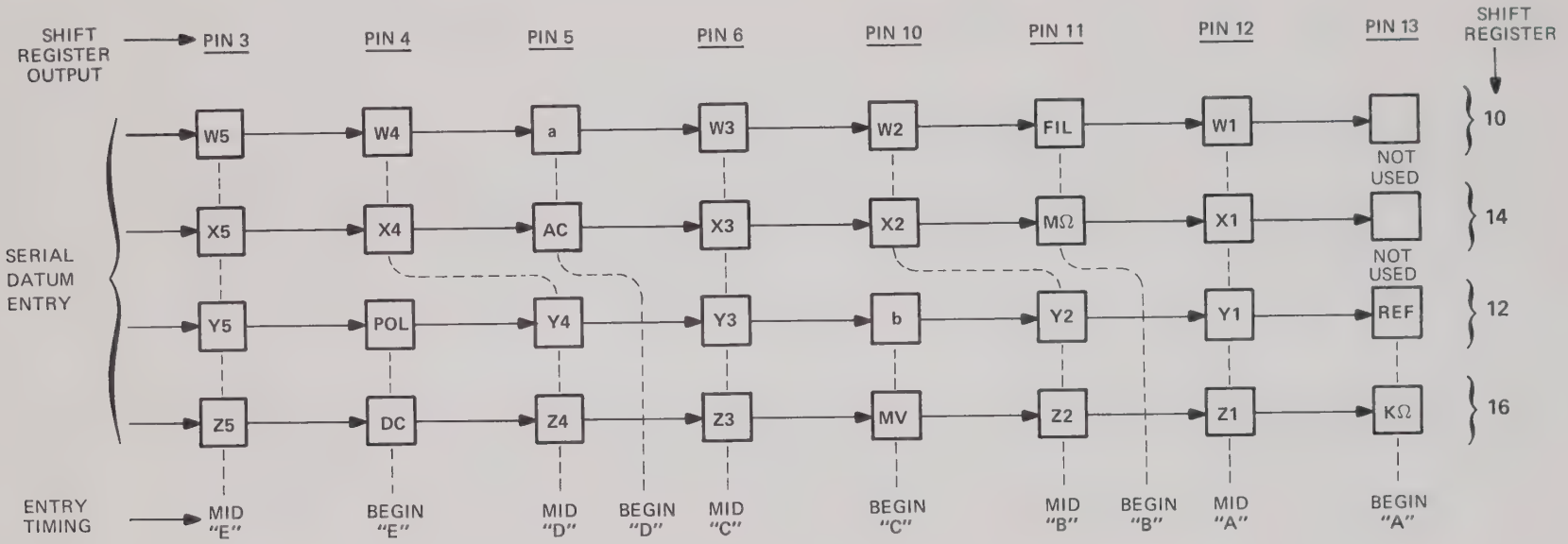


Figure 41. DOU TIMING DIAGRAM



LEGEND: 1. ☐ DENOTES FUNCTION, RANGE, OR DIGIT BIT
2. ENTRY TIMING DESIGNATIONS DENOTE WHEN DATA IS LOADED

Figure 42. SHIFT REGISTER LOAD SEQUENCE (Data Output Unit)

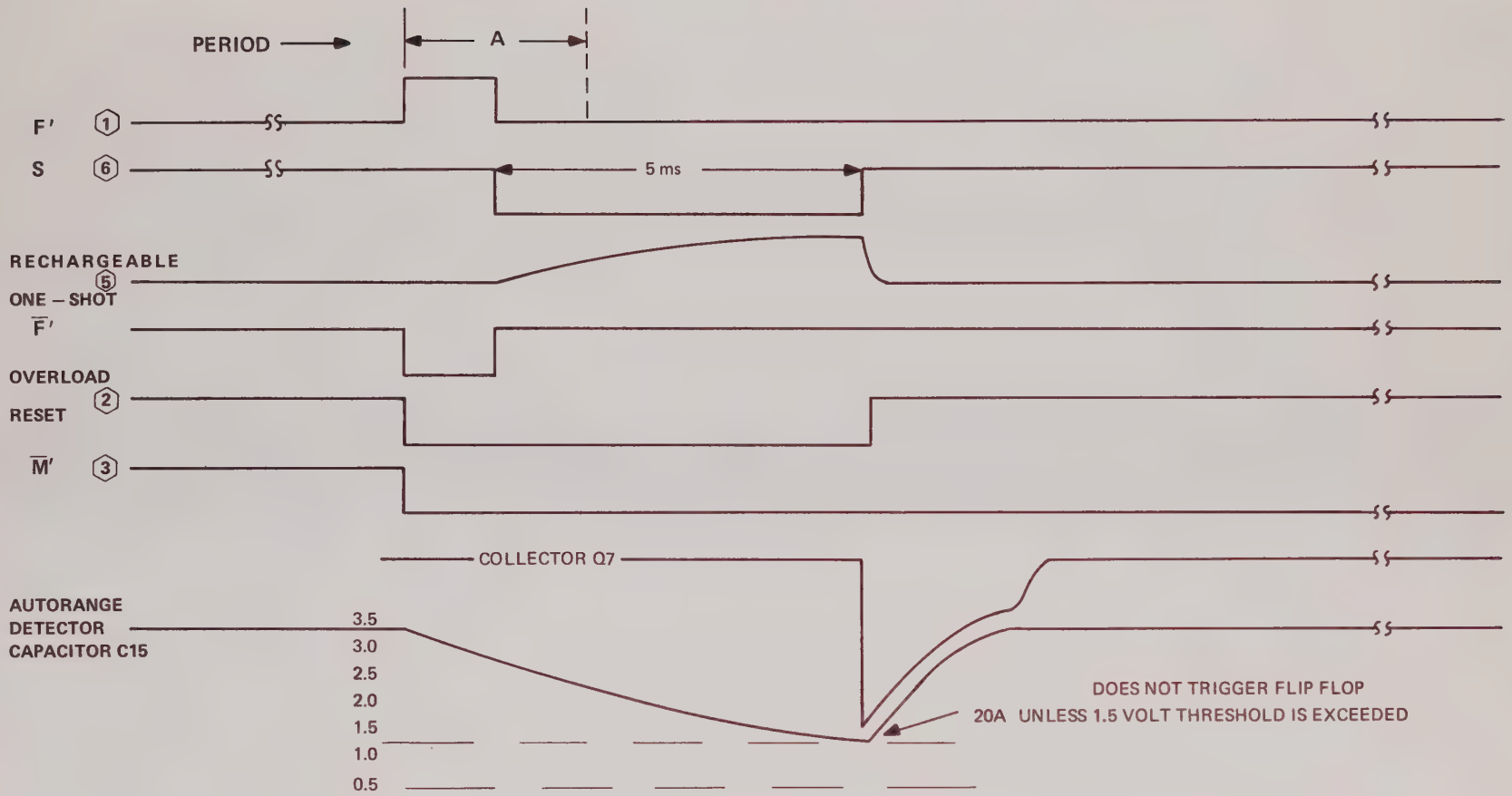


Figure 43. CONTROL SIGNAL TIMING DURING AUTORANGE

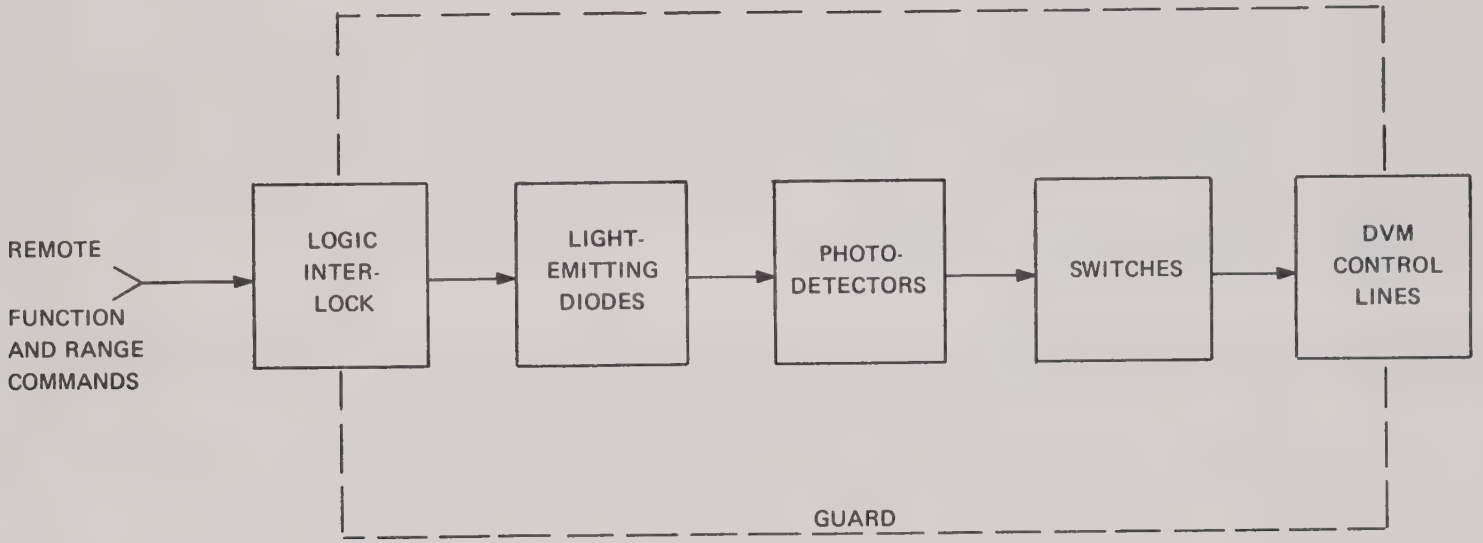
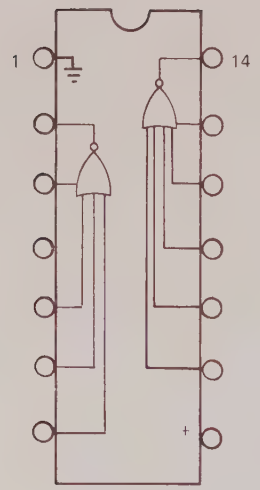
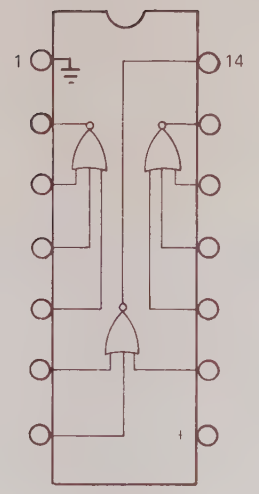


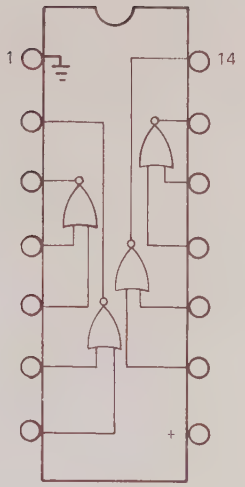
Figure 44. REMOTE CONTROL UNIT BLOCK DIAGRAM



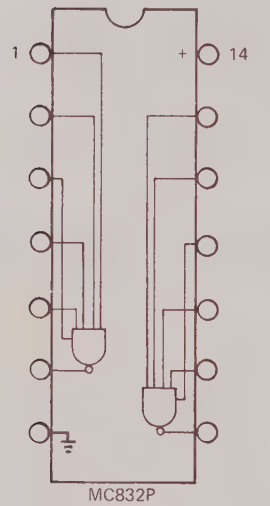
SP317A
JF268557



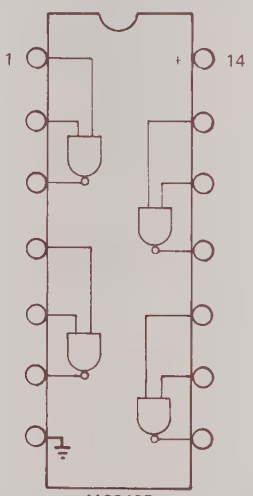
SP370A
JF268565



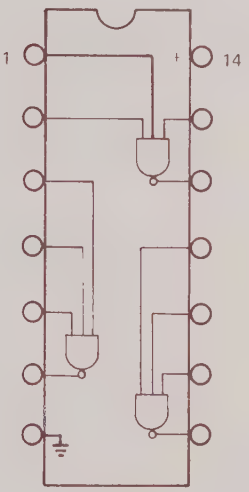
SP380A
JF268540



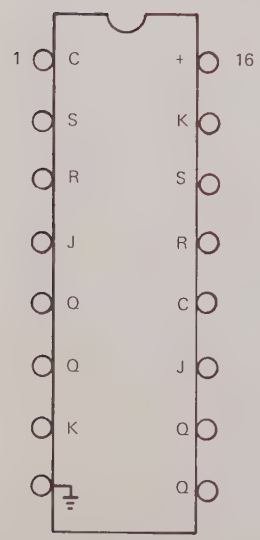
MC832P
JF268383



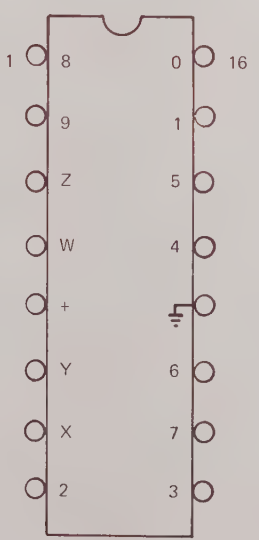
MC846P
JF268375



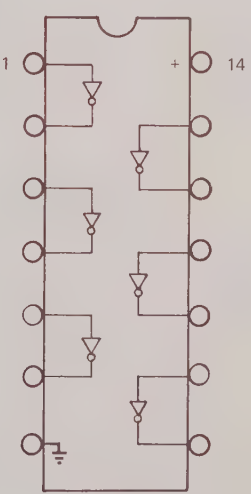
MCP863P
JF266312



SP322B
JF268441



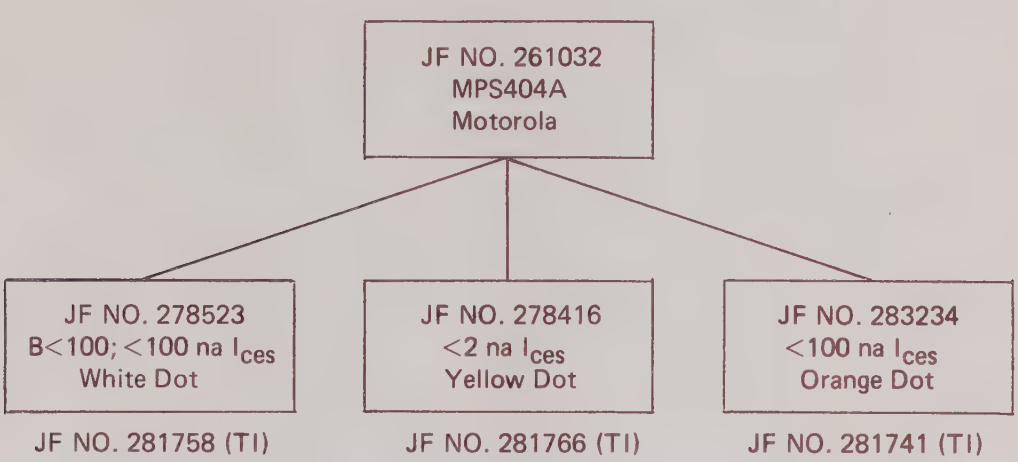
DM8840N
JF267211



836P
JF268367

TOP VIEW

8100A/8300A SELECTED TRANSISTORS



The above selected part numbers are used in the following areas of the 8100 and 8300.

8100A (8)

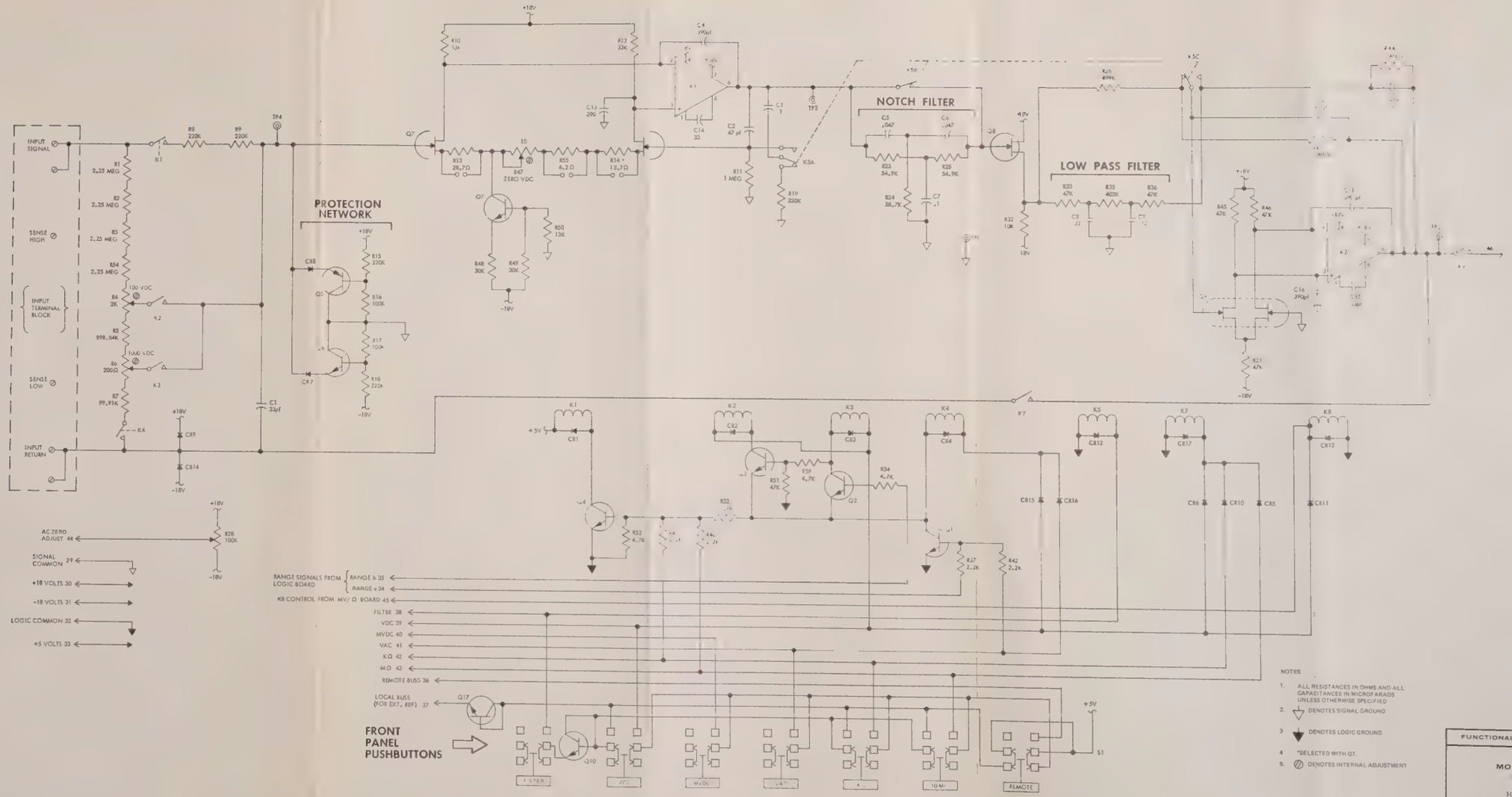
Schematic Designation	Color
Q19	White
Q20	White
Q21	White
Q22	White
Q23	White
Q25	Orange
Q61	Yellow
Q76	Yellow

8300A (6)

Schematic Designation	Color
Q106	Orange
Q107	Orange
Q116	Orange
Q123	Orange

MV/Ω Converter

Q6	Orange
Q7	Orange



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ▽ DENOTES SIGNAL GROUND
3. ▼ DENOTES LOGIC GROUND
4. *SELECTED WITH Q7.
5. ⊘ DENOTES INTERNAL ADJUSTMENT

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
BUFFER

SCHEMATIC NO 1

SER NO 1121 & ON — REV A

FLUKE JOHN FLUKE MFG. CO., INC.
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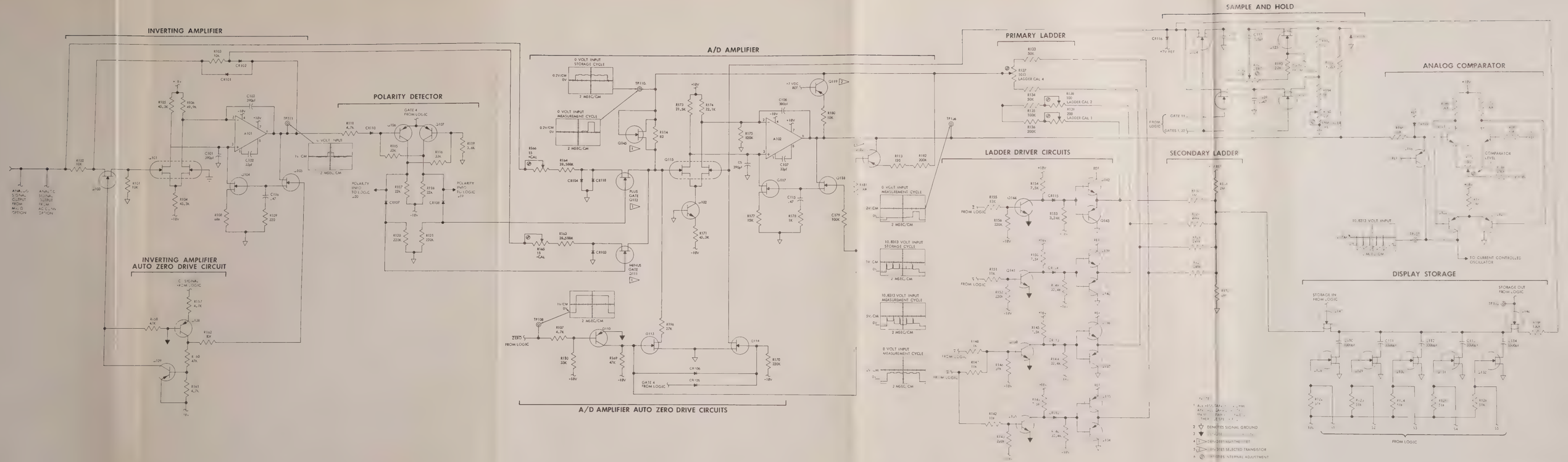


FUNCTIONAL SCHEMATIC DIAGRAM

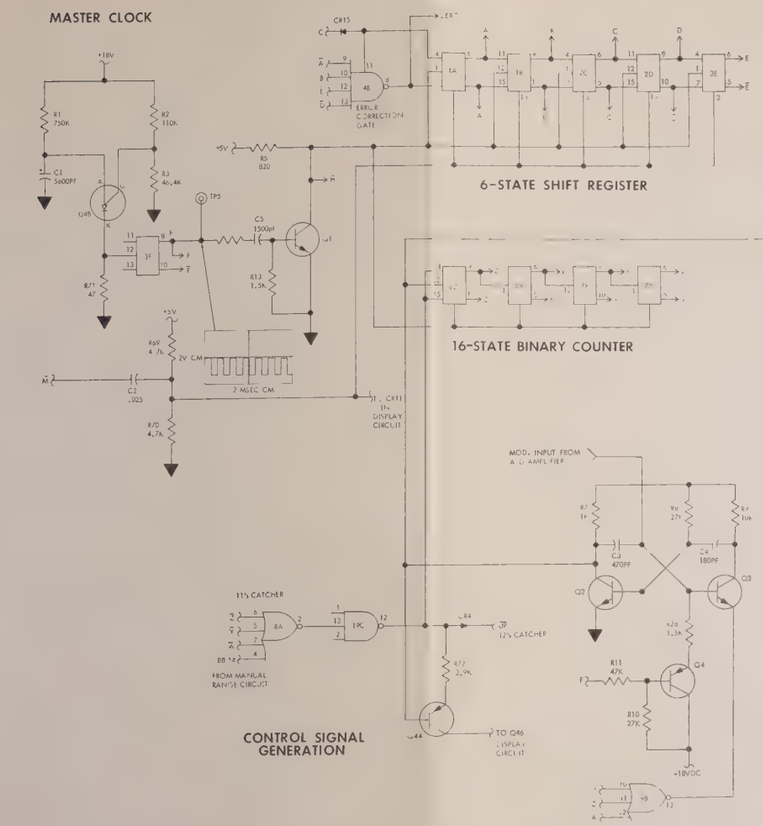
MODEL 8300A
A/D CONVERTER

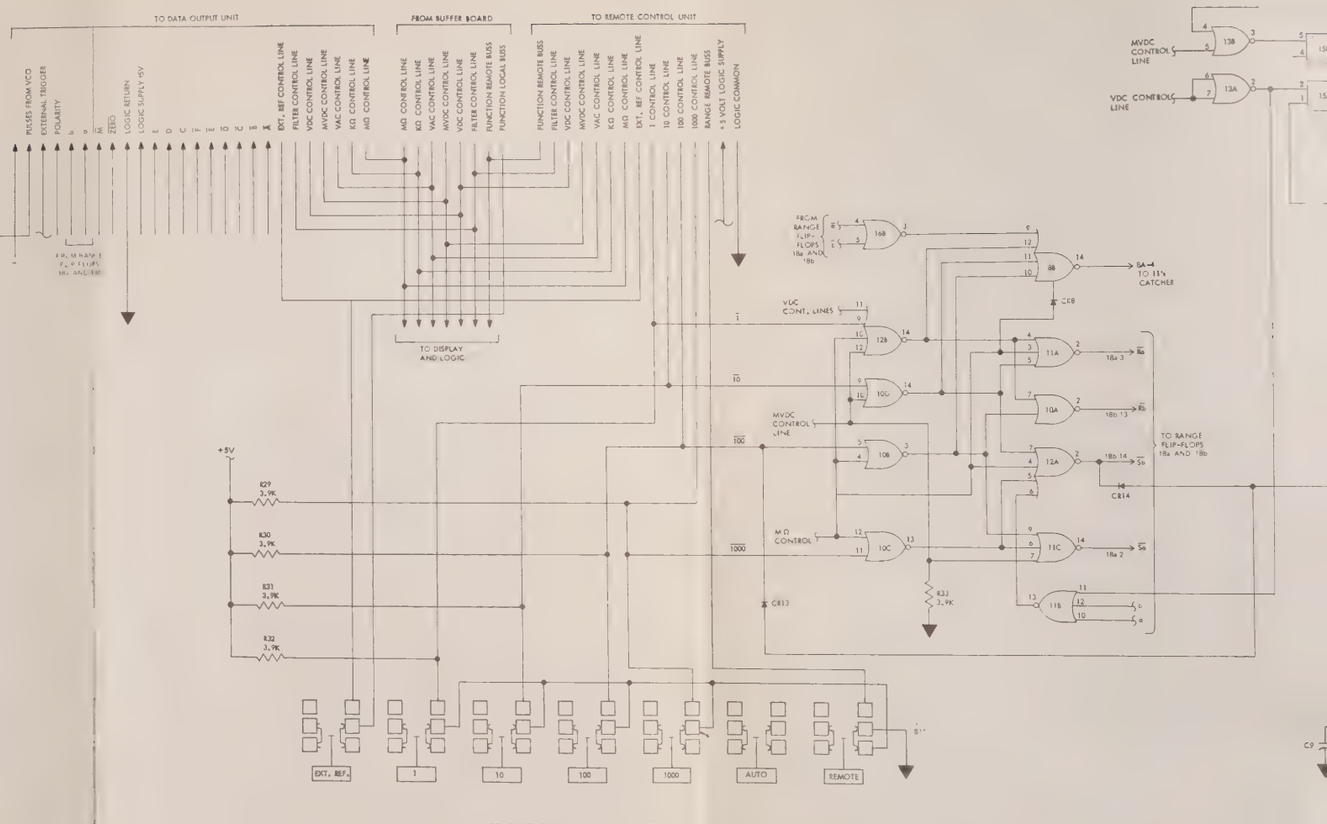
SCHEMATIC NO. 2

SER. NO. 123 & ON

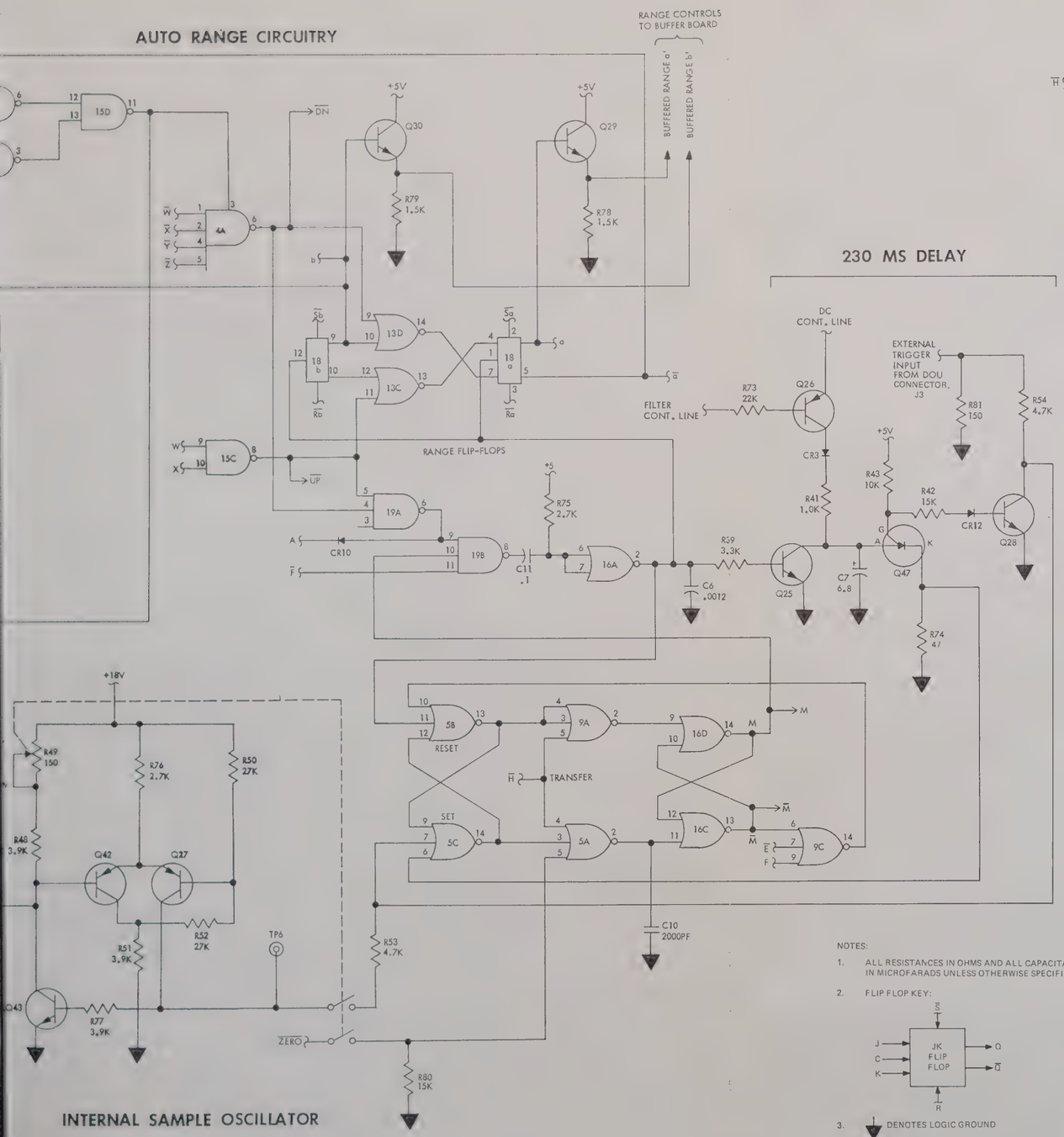
REV
CL

FLUKE JOHN FLUKE MFG CO., INC.
P.O. Box 7428 Seattle Washington 98133


MASTER CLOCK
+18V
R1 750K
R2 R10k
C1 .5600PF
Q45
R3 40.4K
TP5
C5 1500pf
Q1
R13 1.5k
R27 47
+5V
R69 4.7k
2V CM
7 MSEC CM
C2 .025
R70 4.7k
TO CR11 IN DISPLAY CIRCUIT
CR15
ERROR CORRECTION GATE
6-STATE SHIFT REGISTER
R5 820
16-STATE BINARY COUNTER
MOD. INPUT FROM A-C AMPLIFIER
R1 1k
R6 27k
R7 10k
C3 470PF
C4 180PF
Q2
Q3
R26 1.5k
R11 47K
Q4
R10 27K
-18VDC
11% CATCHER
FROM MANUAL RANGE CIRCUIT
CR4
3% 12% CATCHER
R72 2.0k
Q44
TO Q46 DISPLAY CIRCUIT
CONTROL SIGNAL GENERATION
CURRENT CONTROLLED OSCILLATOR


TO DATA OUTPUT UNIT
FROM BUFFER BOARD
TO REMOTE CONTROL UNIT
PULSES FROM VCO
EXTERNAL TRIGGER
POLARITY
ZERO
LOGIC RETURN
LOGIC SUPPLY +5V
EXT. REF CONTROL LINE
FILTER CONTROL LINE
VDC CONTROL LINE
MVDC CONTROL LINE
VAC CONTROL LINE
KΩ CONTROL LINE
MΩ CONTROL LINE
FUNCTION REMOTE BUSS
FUNCTION LOCAL BUSS
1 CONTROL LINE
10 CONTROL LINE
100 CONTROL LINE
1000 CONTROL LINE
RANGE REMOTE BUSS
+5 VOLT LOGIC SUPPLY
LOGIC COMMON
FROM RANGE FLIP-FLOPS 18a AND 18b
TO DISPLAY AND LOGIC
TO 11% CATCHER
TO RANGE FLIP-FLOPS 18a AND 18b
MVDC CONTROL LINE
VDC CONTROL LINE
VDC CONT. LINES
MVDC CONTROL LINE
MΩ CONTROL
CR13
CR14
+5V
R29 3.9K
R30 3.9K
R31 3.9K
R32 3.9K
R33 3.9K
EXT. REF.
1
10
100
1000
AUTO
REMOTE
FRONT PANEL PUSH BUTTONS

AUTO RANGE CIRCUITRY

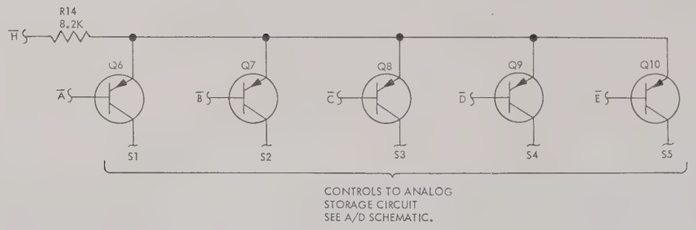


INTERNAL SAMPLE OSCILLATOR

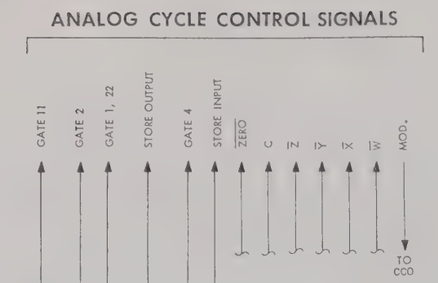
NOTES:

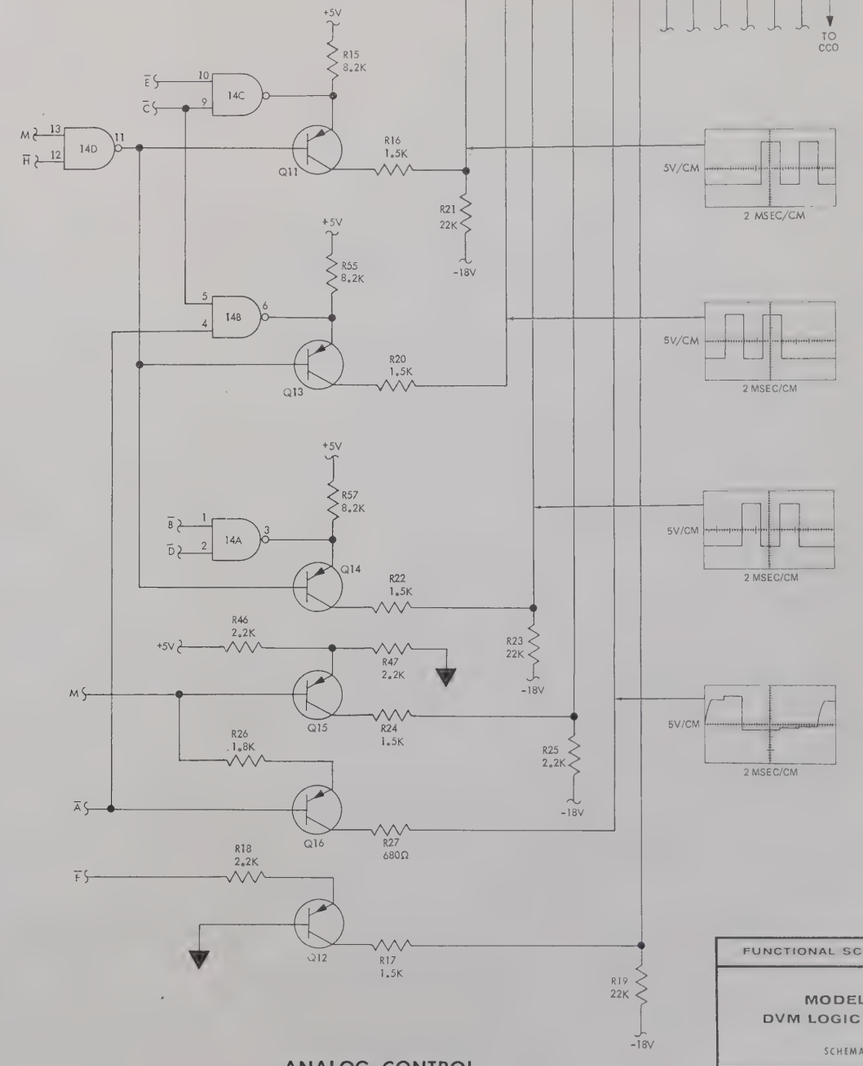
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLIP FLOP KEY:

3. DENOTES LOGIC GROUND
4. * SWITCHES COMPRISING S1 SHOWN IN OFF (NON DEPRESSED) POSITION.



ANALOG CYCLE CONTROL SIGNALS





ANALOG CONTROL

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
DVM LOGIC & CONTROL

SCHEMATIC NO. 3

SER. NO. 123 & ON

REV. a

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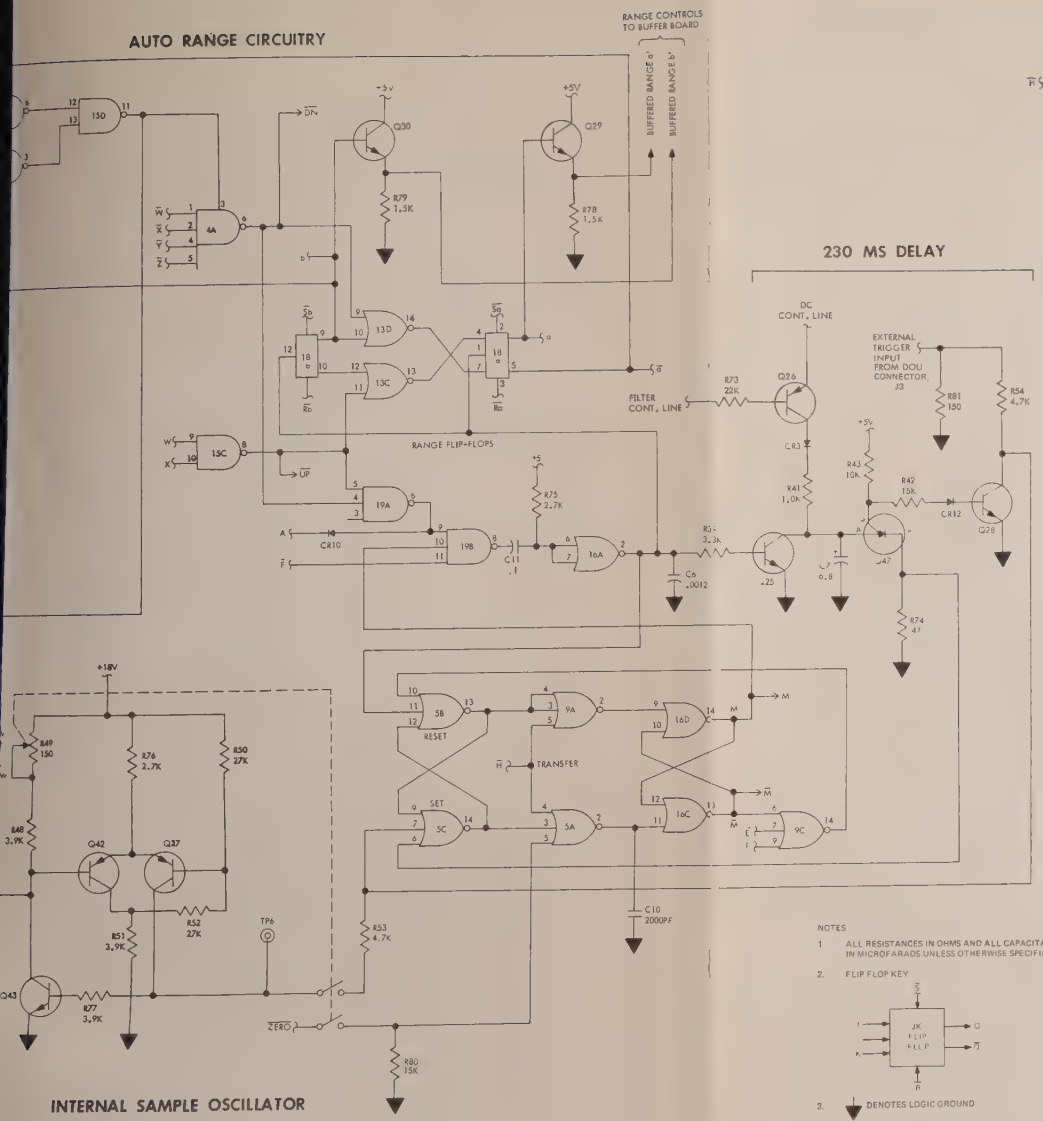
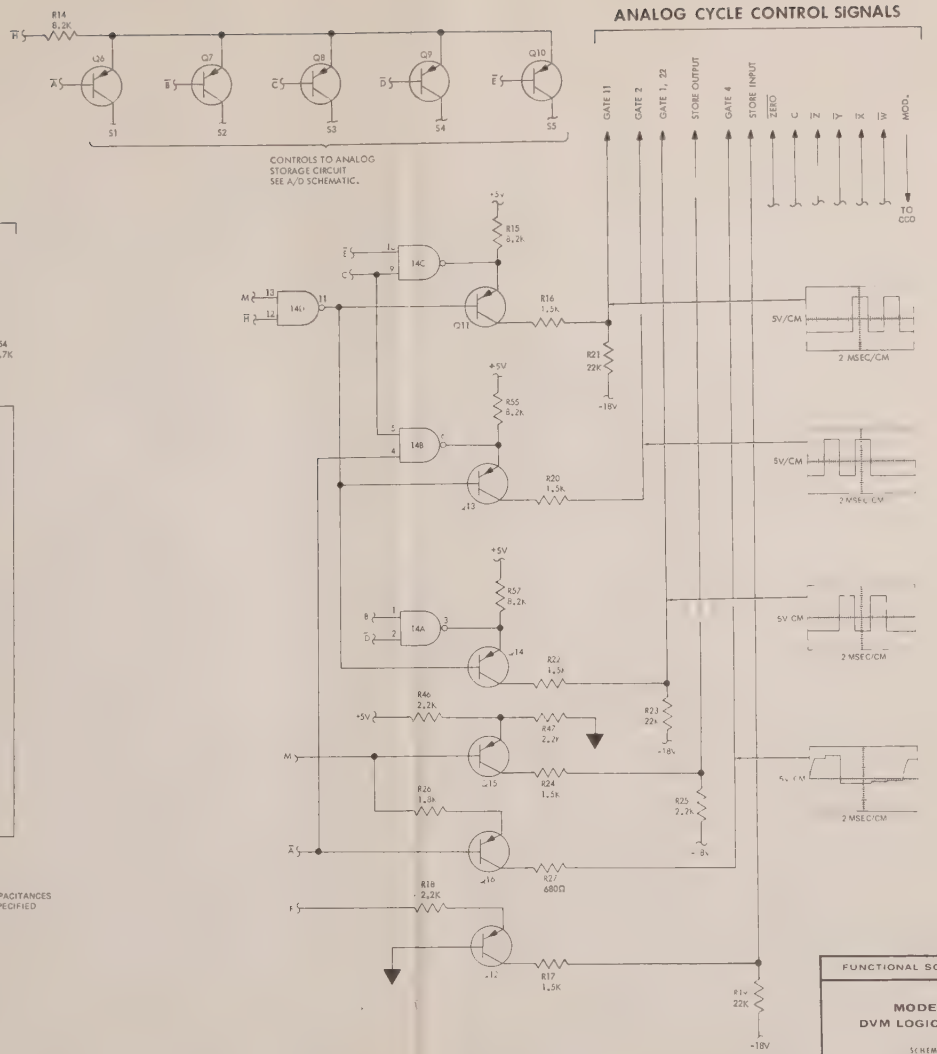


NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. FLIP FLOP KEY

3. DENOTES LOGIC GROUND
4. ◆ SWITCHES COMPRISING S1 SHOWN IN OFF (NON DEPRESSED) POSITION



FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
DVM LOGIC & CONTROL

SCHEMATIC NO 3

SER NO 123 & ON | REV 0

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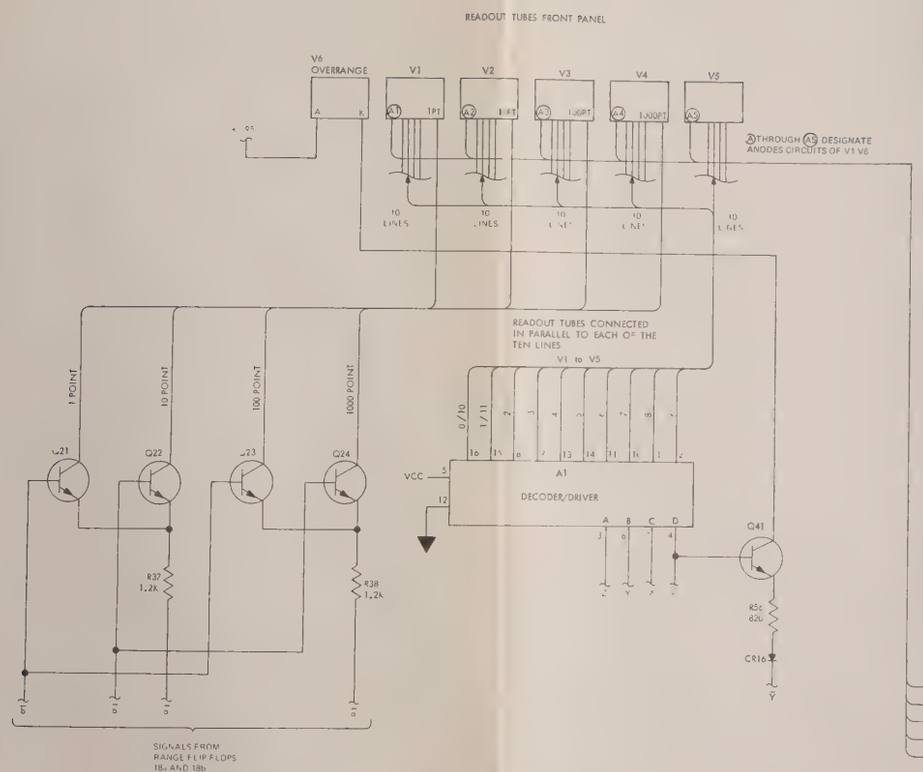
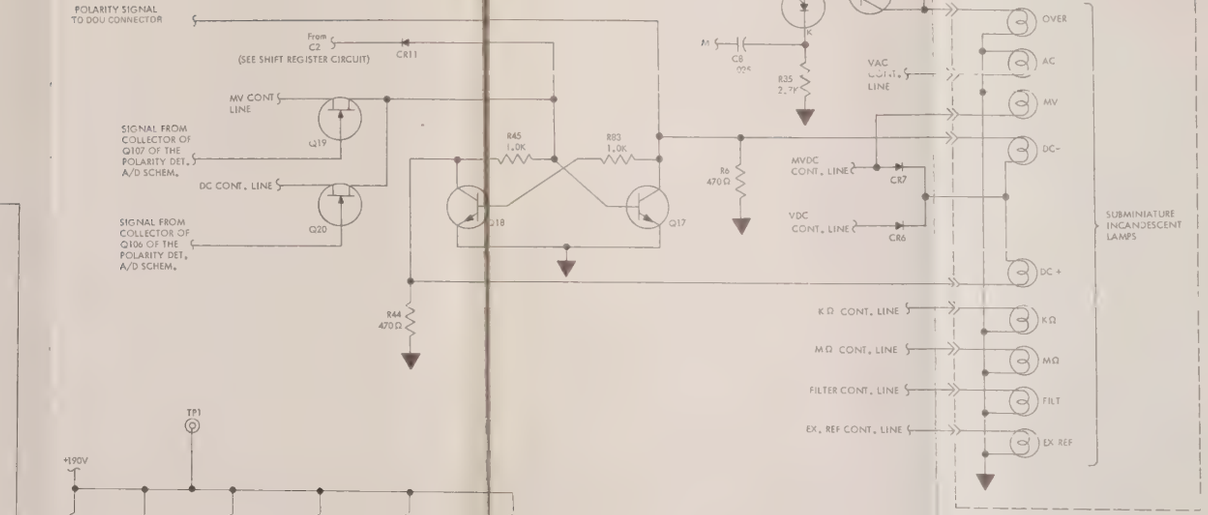
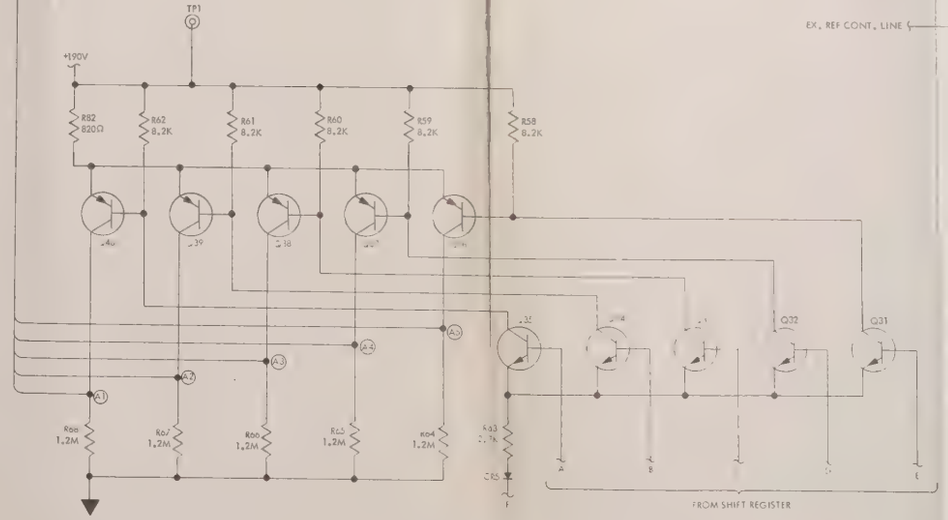
DISPLAY CIRCUITRY







ANODE STROBING CONTROL

NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC GROUND

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DISPLAY	
SCHEMATIC NO. 4	
SER NO 21 & ON	REV 12
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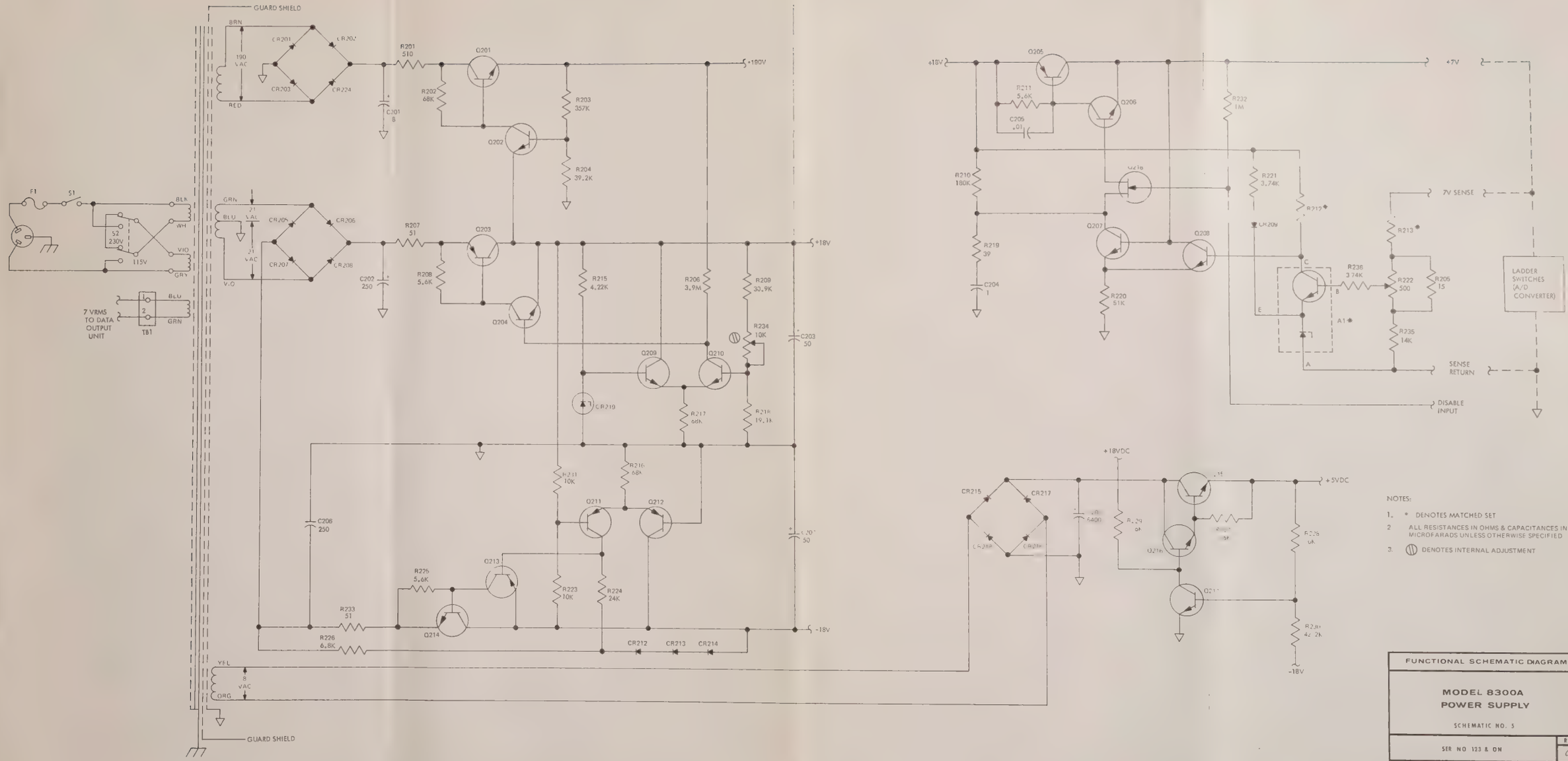

NOTES:

1. * DENOTES MATCHED SET
2. ALL RESISTANCES IN OHMS & CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
3. (II) DENOTES INTERNAL ADJUSTMENT

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
POWER SUPPLY

SCHEMATIC NO. 5

SER NO 123 & ON	REV. a

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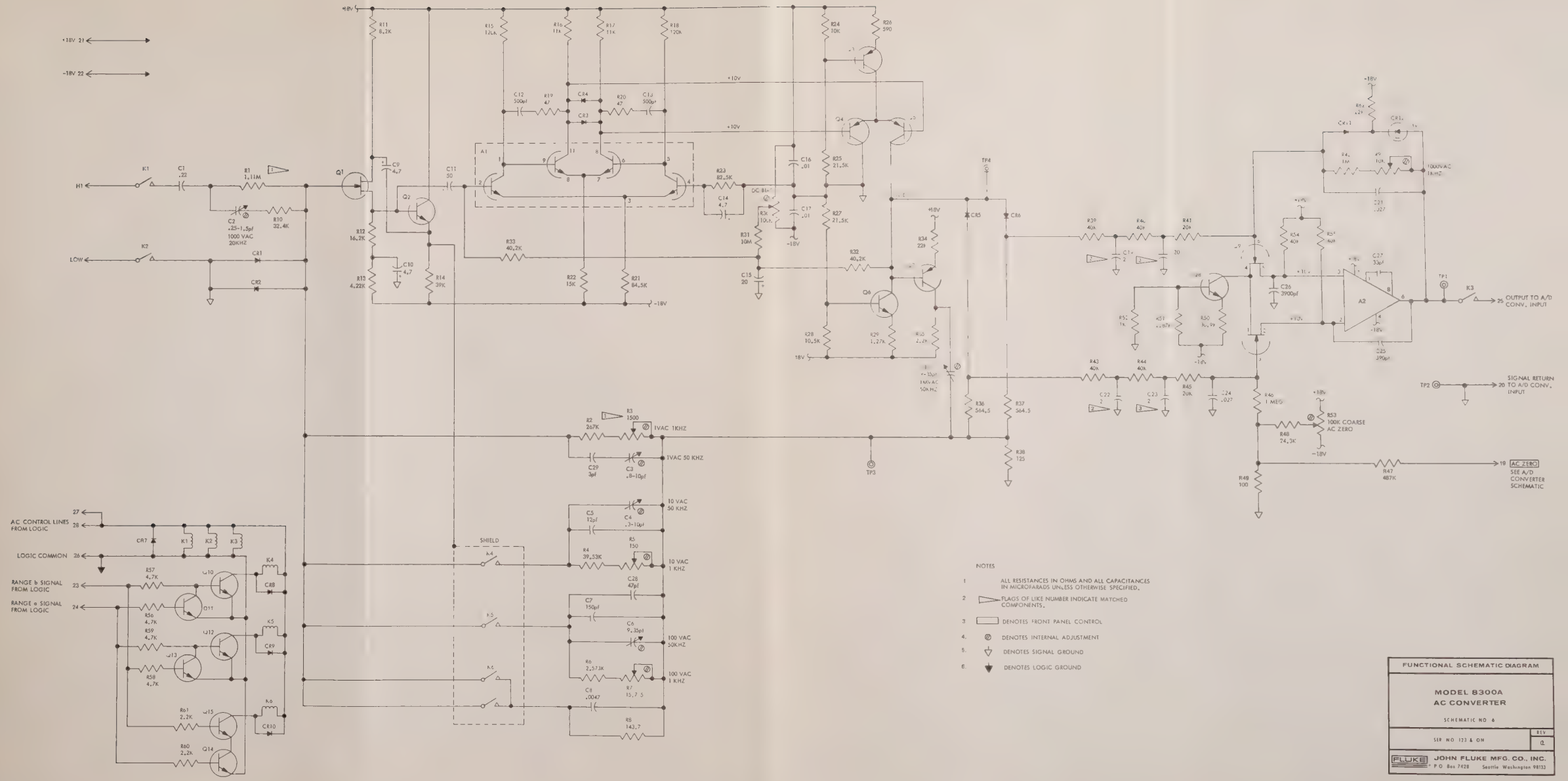

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
AC CONVERTER

SCHEMATIC NO 6

SER NO 173 & ON

REV
C

FLUKE JOHN FLUKE MFG. CO., INC.
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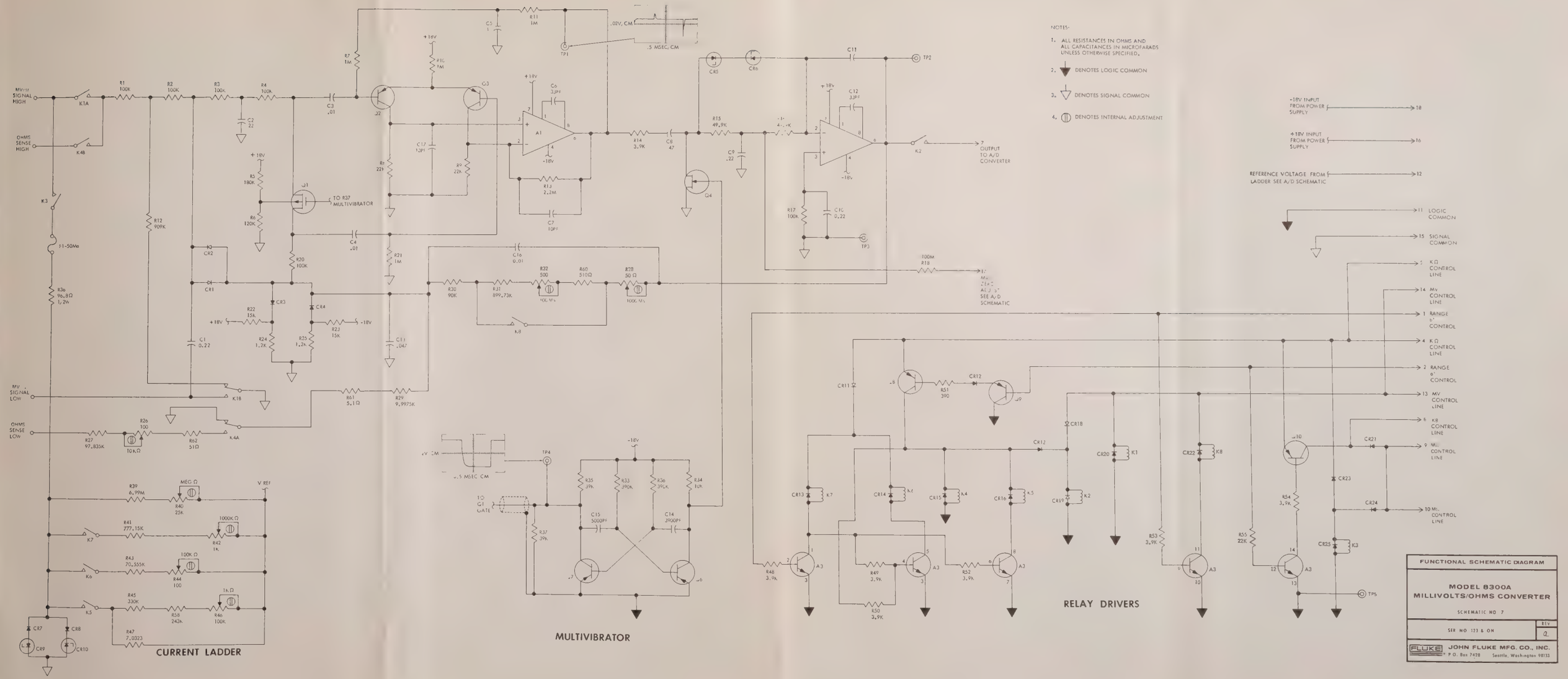
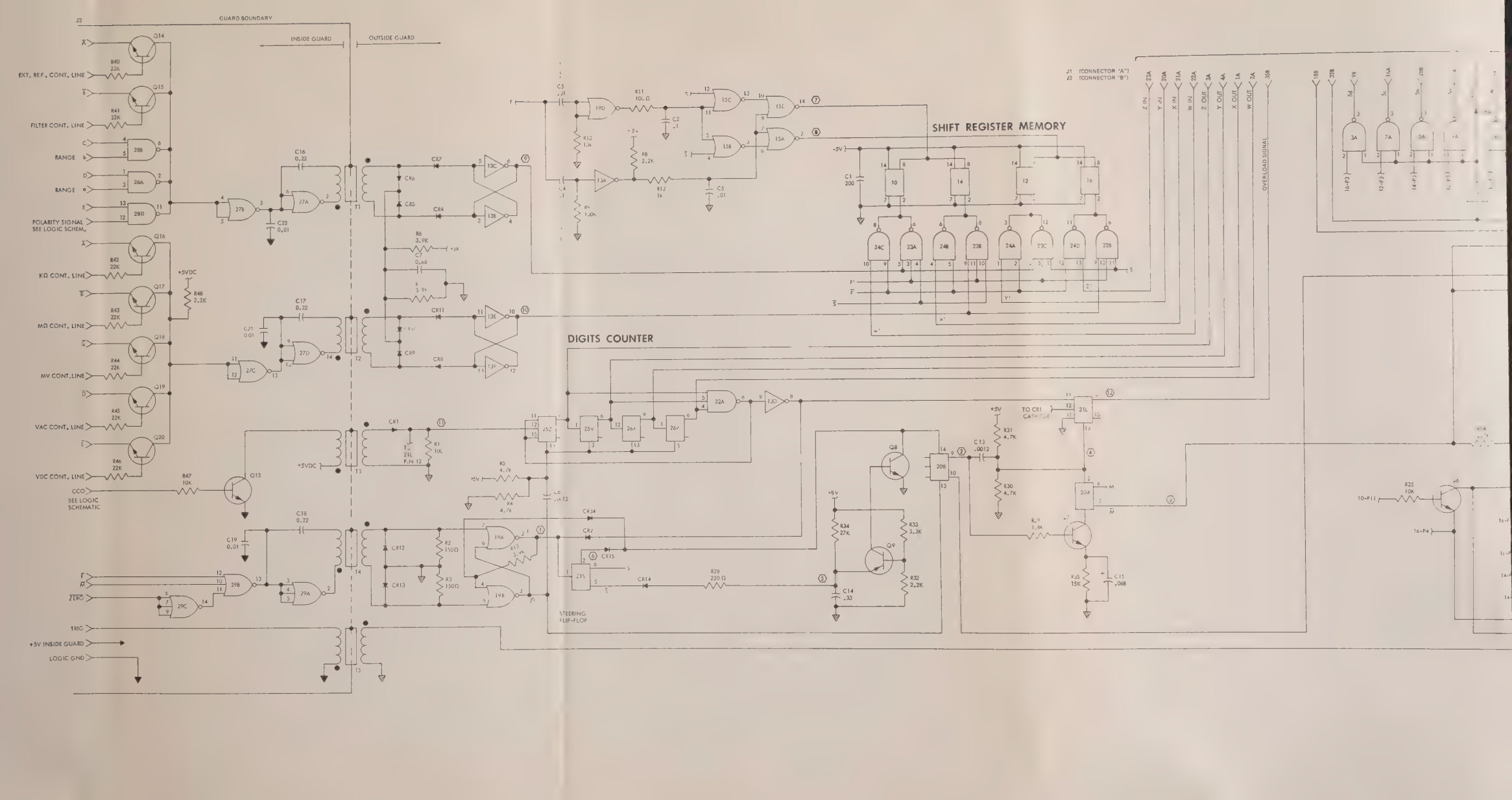
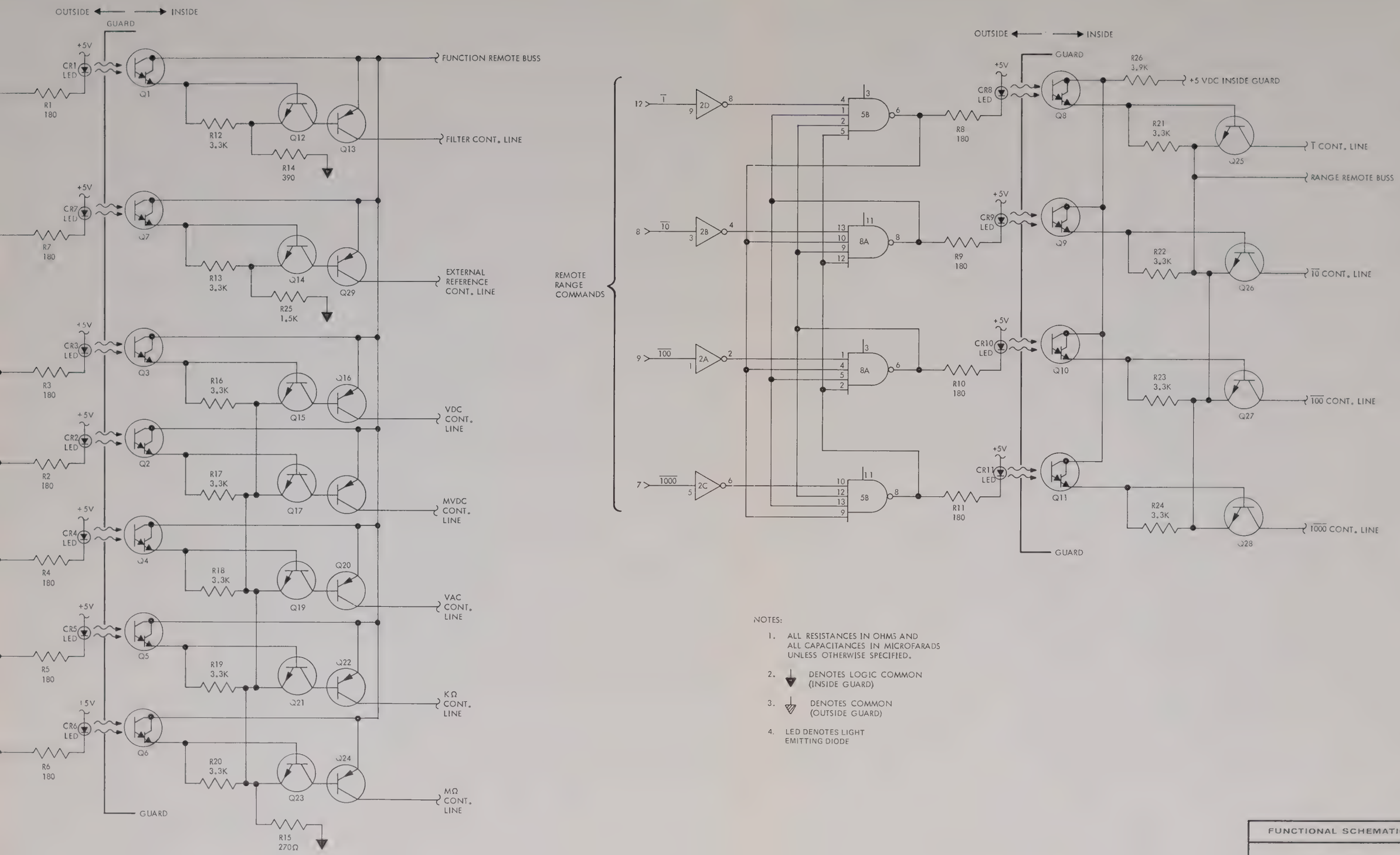

NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. DENOTES LOGIC COMMON
3. DENOTES SIGNAL COMMON
4. DENOTES INTERNAL ADJUSTMENT
-18V INPUT FROM POWER SUPPLY
+18V INPUT FROM POWER SUPPLY
REFERENCE VOLTAGE FROM LADDER SEE A/D SCHEMATIC
11 LOGIC COMMON
15 SIGNAL COMMON
5 KΩ CONTROL LINE
14 MV CONTROL LINE
1 RANGE b' CONTROL
4 KΩ CONTROL LINE
2 RANGE a' CONTROL
13 MV CONTROL LINE
6 K8 CONTROL LINE
9 MΩ CONTROL LINE
10 MΩ CONTROL LINE
MV SIGNAL HIGH
OHMS SENSE HIGH
MV SIGNAL LOW
OHMS SENSE LOW
K1A
K48
K3
K18
K4A
F1-50Ma
R1 100K
R2 100K
R3 100K
R4 100K
R12 909K
R26 100
R27 97.835K
R62 51Ω
R61 5.1Ω
R29 9.9975K
R30 90K
R31 899.73K
R32 500
R60 510Ω
R28 50Ω
100K MΩ
R18 100M
TO A/D SCHEMATIC
OUTPUT TO A/D CONVERTER
TO R37 MULTIVIBRATOR
TP1
TP2
TP3
TP4
TP5
.02V/CM
.5 MSEC/CM
TO G1 GATE
CURRENT LADDER
MULTIVIBRATOR
RELAY DRIVERS
FUNCTIONAL SCHEMATIC DIAGRAM
MODEL 8300A
MILLIVOLTS/OHMS CONVERTER
SCHEMATIC NO 7
SER NO 123 & ON
REV 0
JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


J3
GUARD BOUNDARY
INSIDE GUARD
OUTSIDE GUARD
EXT. REF. CONT. LINE
FILTER CONT. LINE
RANGE
RANGE
POLARITY SIGNAL SEE LOGIC SCHEM.
KΩ CONT. LINE
MΩ CONT. LINE
MV CONT. LINE
VAC CONT. LINE
VDC CONT. LINE
CCO SEE LOGIC SCHEMATIC
ZERO
TRIG
+5V INSIDE GUARD
LOGIC GND
+5VDC
SHIFT REGISTER MEMORY
DIGITS COUNTER
STEERING FLIP-FLOP
OVERLOAD SIGNAL
J1 (CONNECTOR "A")
J2 (CONNECTOR "B")
Z IN
Y IN
X IN
W IN
Z OUT
Y OUT
X OUT
W OUT
TO CR1 CATHODE



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ⏚ DENOTES COMMON (OUTSIDE GUARD)
4. LED DENOTES LIGHT EMITTING DIODE

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
REMOTE CONTROL UNIT

SCHEMATIC NO. 9

SER. NO. 123 & ON | REV 2

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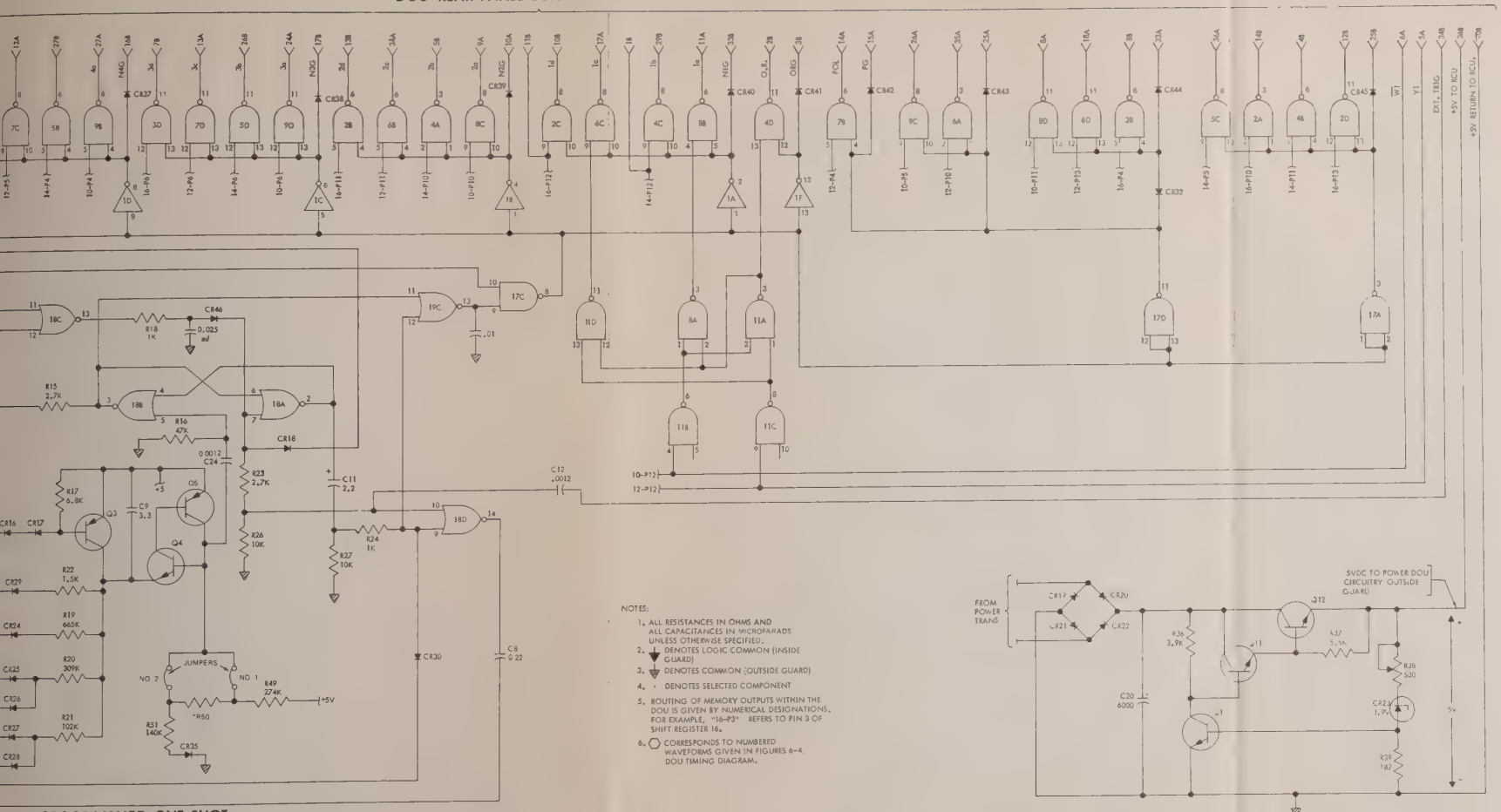
DOU REAR PANEL CONNECTORS



PROGRAMMED ONE SHOT

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ▽ DENOTES COMMON (OUTSIDE GUARD)
4. • DENOTES SELECTED COMPONENT
5. ROUTING OF MEMORY OUTPUTS WITHIN THE DOU IS GIVEN BY NUMERICAL DESIGNATIONS. FOR EXAMPLE, "16-P3" REFERS TO PIN 3 OF SHIFT REGISTER 16A.
6. ◯ CORRESPONDS TO NUMBERED WAVEFORMS GIVEN IN FIGURES 6-4, DOU TIMING DIAGRAM.

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
DATA OUTPUT UNIT

SCHEMATIC NO 8

SER NO 123 & ON | REV a

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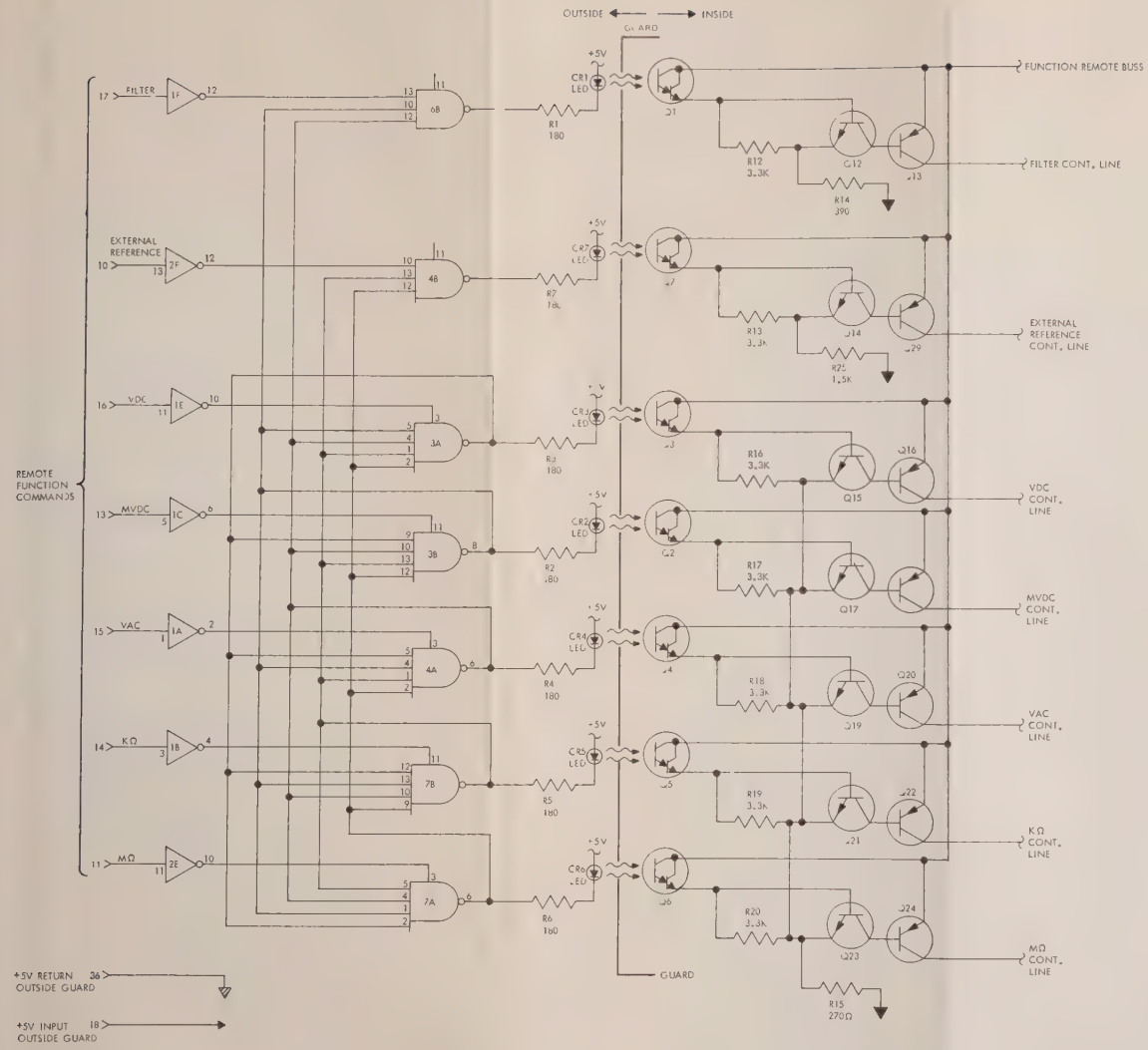
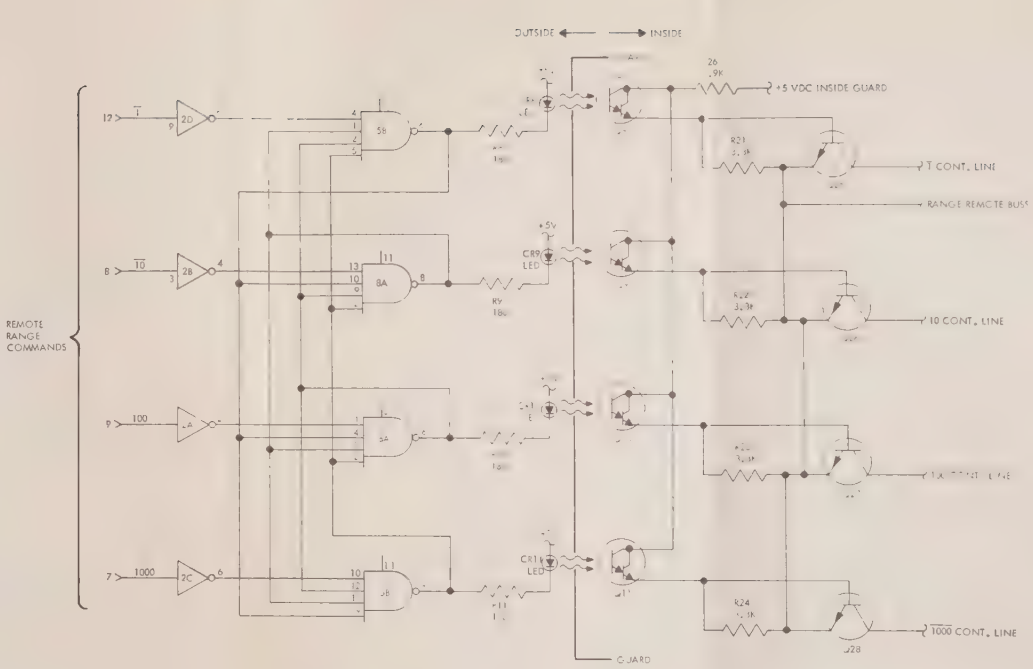
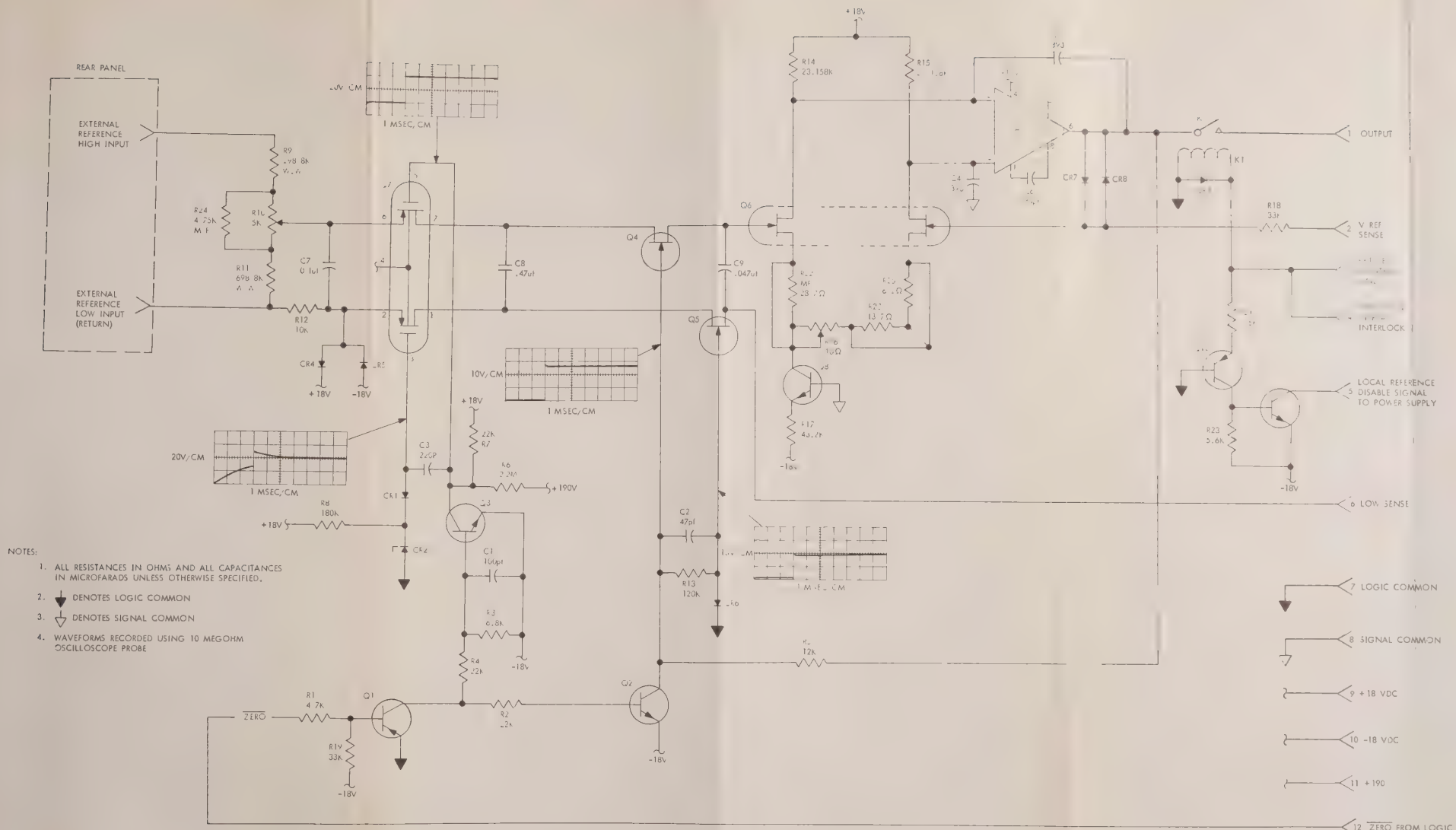




NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ▽ DENOTES COMMON (OUTSIDE GUARD)
4. LED DENOTES LIGHT EMITTING DIODE

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A REMOTE CONTROL UNIT	
SCHEMATIC NO 9	
SER NO 123 & ON	REV 2
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle Washington 98133	



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ▽ DENOTES SIGNAL COMMON
4. WAVEFORMS RECORDED USING 10 MEGOHM OSCILLOSCOPE PROBE

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
EXTERNAL REFERENCE UNIT

SCHEMATIC NO. 10

SER NO. 123 & ON | REV a

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133

ERRATA

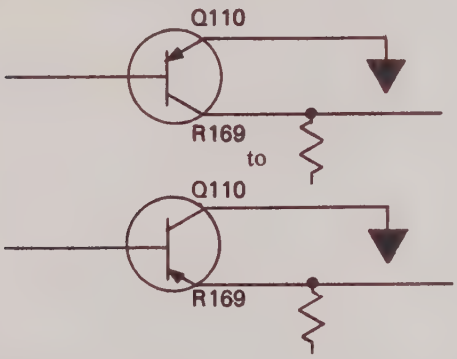
FLUKE MODEL 8300A SCHEMATICS

Schematic No. 1, Buffer

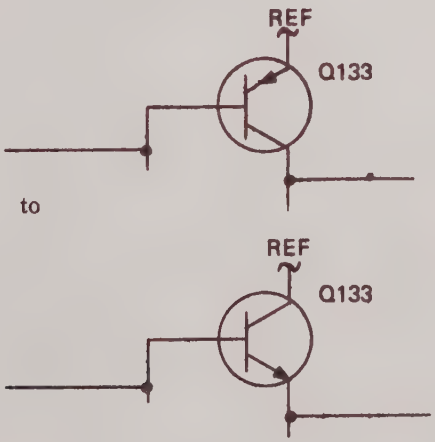
1. Change reference designation Q17 to Q12.

Schematic No. 2, A/D Converter

1. R162 should be 100k.
2. R119 should be 5.6k.
3. Change Q110 circuit from



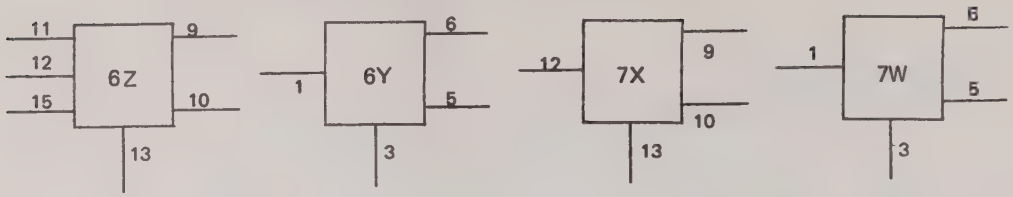
4. R153 should be 32.4k.
5. Change reference designation Q135 to Q155.
6. Change Q133 circuit from



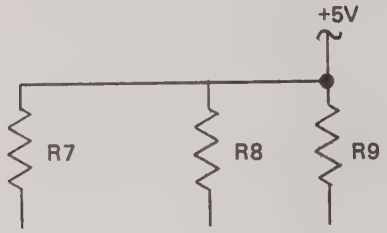
Schematic No. 3, DVM Logic and Control

1. Add reference designation and value to resistor located between test point TP5 and capacitor C5:

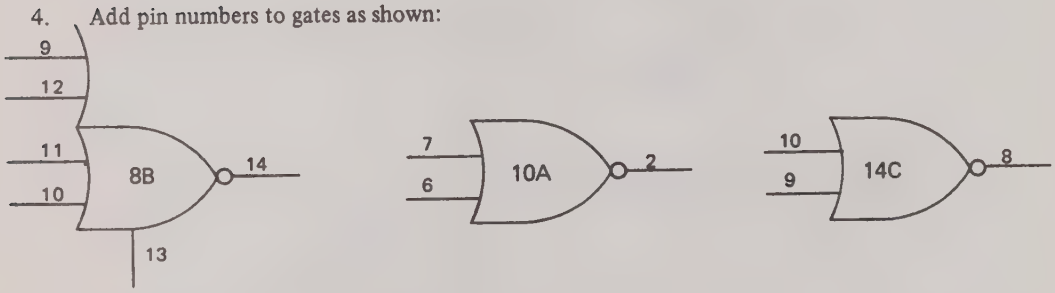
2. Add pin numbers to binary counter flip flops as shown:



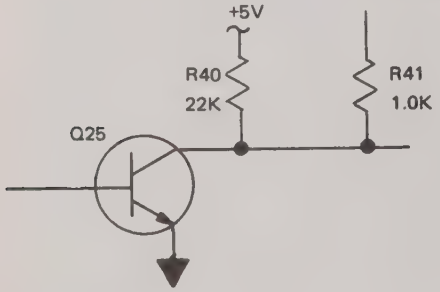
3. Add +5 volt line to junction of R7, R8, and R9:



4. Add pin numbers to gates as shown:



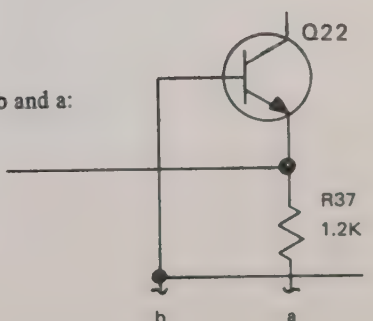
5. R51 should be 2.7k.
6. Add +5 volts through resistor to Q25 collector:



7. R25 should be 22k.

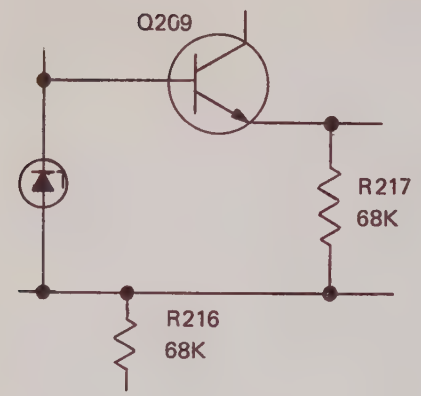
Schematic No. 4, Display

1. Change designations of input signals to Q22 from $\overline{b}$ and $\overline{a}$ to b and a:

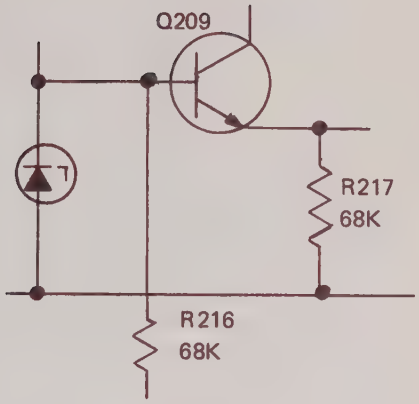


Schematic No. 5, Power Supply

1. Change circuitry from:



to:

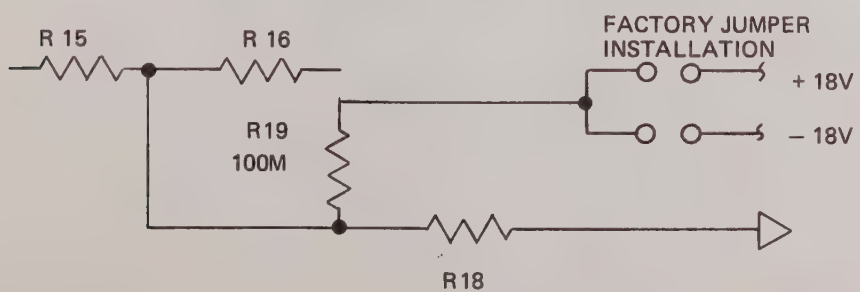


Schematic No. 6, AC Converter

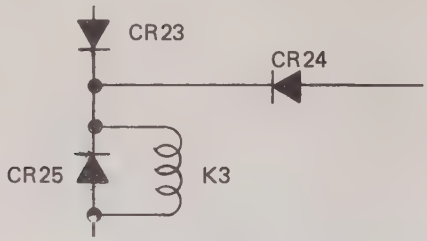
1. C4 should be 0.8 – 10 pf.
2. C6 should be 9 – 35 pf.
3. R7 should be 15Ω.
4. C26 should be 390 pf.

Schematic No. 7, Millivolt/Ohms Converter

1. R3 should be 220k.
2. C2 should be 0.1 uf.
3. Change R62 51Ω to R60 22Ω.
4. Change R61 5.1Ω to R59 4.7Ω.
5. C13 should be 0.1 uf.
6. Change R60 510Ω to R61 240Ω.
7. R33 should be 715k.
8. R36 should be 715k.
9. C15 should be 5600 pf.
10. C14 should be 4700 pf.
11. C11 should be 2.2 uf.
12. Add the following circuitry at the junction of R18 and R16, as shown:

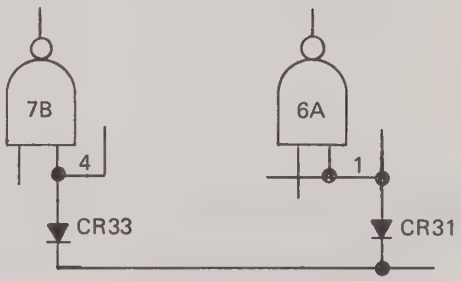


13. Change reference designation of CR12 to CR17.
14. Change circuitry of CR23 as shown:



Schematic No. 8, Data Output Unit

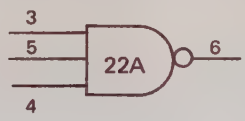
1. C15 should be 0.68 uf.
2. R21 should be 100k.
3. Reference designation of .01 uf capacitor at pin 9 of gate 17C is C10.
4. Add diodes CR31 and CR33 as shown:

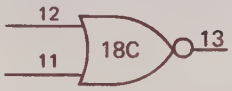


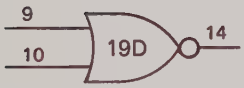
5. Correct/add signal designations for connector pins as shown in following table:

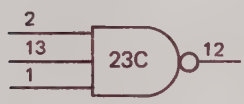
Pin/Connector	Signal Designation
15B	N5G
6B	4d
12A	4c
27B	4b
11B	$\overline{Z1}$
1B	$\overline{X1}$
26A	a
35A	b
8A	FILTER
18A	EXT REF
8B	DC
33A	FIG
36A	AC
14B	MV
4B	MΩ
12B	KΩ
25B	F2G

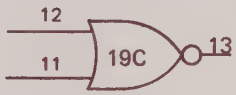
6. Connector pin designation of "+5V RETURN TO RCU" should be 30B.
7. Add/correct pin numbers of components as shown:

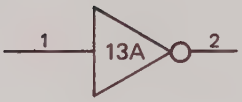


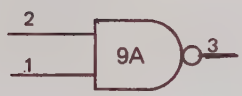






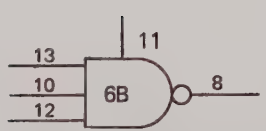


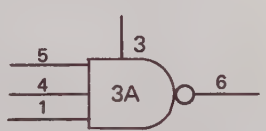


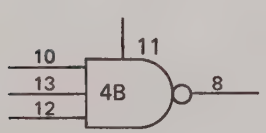


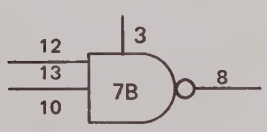
Schematic No. 9, Remote Control Unit

1. R14 should be 270Ω.
2. R25 should be 820Ω.
3. R15 should be 180Ω.
4. Add missing transistor reference designation, Q18.
5. Add output pin numbers to NAND gates as shown:









1970 PRODUCT DIRECTORY

JOHN FLUKE MFG. CO., INC.

FLUKE®

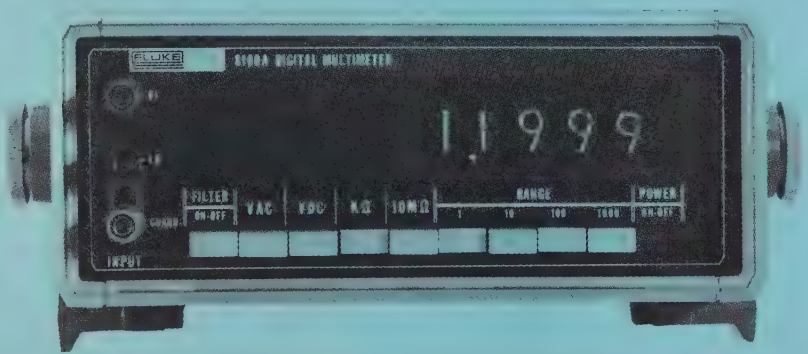
NEW-NEW-NEW

A New Approach to Digital Voltmeters

The new Fluke family of digital voltmeters uses circuit disciplines never before adapted to this kind of instrumentation. The Models 8100A and 8300A offer an analog to digital conversion technique based on storage capacitors, a single BCD counter and a resistive ladder network to serially determine and display all digits. The technique is called Recirculating Remainder A to D conversion.

The Model 8100A Digital Multimeter features four full digits plus "1" for 20% overranging; rechargeable battery operation; push-button selectable functions; four range measurement for AC and DC to 1200 volts and five range measurement in ohms.

The Model 8300A Digital Voltmeter features five full digits plus "1" for 20% overranging; auto ranging; 25 millisecond sampling speed; full systems capability with timing signals and ready indicator, low cost options including AC voltage, millivolt/ohms, isolated external reference (4 terminal ratio) fully isolated remote programming and data output, and AC/AC ratio.



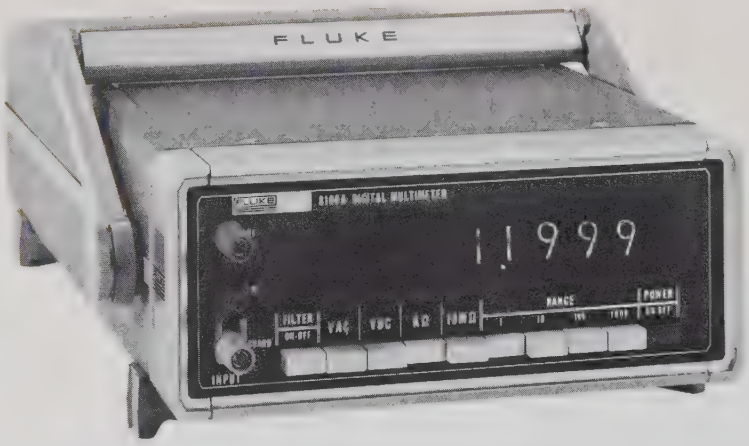
Model 8100A (Page 2)

Model 8300A (Page 3)

Table of Contents

Calibrators	
DC Voltage	5
Meter	8
Programmable Voltage/Current	4
Voltage/Current	8
Calibration Systems	9
Electronic Galvanometers	10
Frequency Comparators	11
Frequency Distribution Amplifier	11
Frequency Synthesizers	10, 11
Multimeters	
Differential	7
Digital	2
Null Detector Microvoltmeter	8
Omega Commutator	11
Power Supplies	
High Voltage	9
Nims High Voltage	5
Rack Mounting Configurations	6
Ratio Measurement Devices	9
Thermal Transfer Standard	7
Transit Cases	7
VAW Meter	12
VLF Receiver/Comparator	11
Voltage Dividers	7
Voltmeters	
Differential	6
Digital	3
RMS Differential	7
RMS Digital	7

DIGITAL MULTIMETER-MODEL 8100A



MODEL 8100A 0.02% DIGITAL MULTIMETER HAS COMPLETE PORTABILITY

- Measures AC and DC volts in four ranges to 1200 volts
- Measures ohms in five ranges to twelve megohms
- Optional rechargeable battery pack operation
- Automatic polarity indication
- All functions are push-button selectable
- Active 2-pole switchable filter
- Four full digits plus "1" for 20% overranging
- Meets specifications for 90 days from 15°C to 35°C, and 0 to 80% relative humidity
- New conversion method reduces power consumption.

SPECIFICATIONS

GENERAL

Size:	3½" high x 8½" wide x 15" deep
Power:	115/230 VAC±10%, 50 to 500 Hz. 10 watts 8 hours operation on optional batteries
Weight:	10.5 lbs. with batteries
Price:	Full multimeter, $695
Option	01—rechargeable battery power, $100
Accessories:	■ HF probe ■ HV probes ■ Switched AC-DC current shunts ■ Ruggedized case ■ Rack mounting brackets

DC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy:	±(0.05% of reading + 0.01% of range)
30 Days:	±(0.02% of reading + 0.01% of range) 20°C to 30°C
Input Impedance:	10 megohms all ranges at all times
Speed:	0.5 sec without filter 1.0 sec with filter
Common Mode Rejection Ratio:	> 100 db DC to 60 Hz with filter (Infinite when battery operated.)
Normal Mode Rejection Ratio:	50 db at 60 Hz with filter

AC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy:	±(0.2% reading + 0.05% of range) 50 Hz to 10 KHz ±(0.5% reading + 0.05% of range) 30 Hz to 50Hz, 10 KHz to 20 KHz
Speed:	< 3.0 sec
Input Impedance:	1 megohm paralleled with < 30 pf.

OHMS

Ranges:	1K, 10K, 100K, 1M, 10M
Accuracy:	±(0.1% reading + 0.01% of range)
Speed:	0.5 secs thru 1 megohm without filter 3.0 secs 10 megohm without filter
Voltage Across Unknown R:	1V at full scale decreasing linearly to 0 volts.

DIGITAL VOLTMETER-MODEL 8300A

Model 8300A 0.005% DIGITAL VOLTMETER HAS TOTAL BUILT-IN SYSTEMS CAPABILITY

- Basic unit measures 0 to 1100 volts DC in three ranges
- New conversion method for increased reliability
- Reads out in five full digits plus "1" for 20% overranging
- 25 millisecond sampling speed
- Automatic ranging and polarity
- Fully guarded with 140 db common mode rejection
- Active 3 pole switchable filter with 60 Hz notch
- Normal Mode Rejection Ratio 60 db, 50 Hz and up
- Full systems capability with timing signals, ready indicators and flags
- DTL-TTL compatible Data Output and Programming
- Meets all 90 day specifications from 20°C to 30°C, and 0 to 70% RH.

WITH LOW COST OPTIONS, TAILOR THE FLUKE 8300A DVM TO YOUR EXACT SYSTEM REQUIREMENT.

- AC voltage measurement in four ranges 0 to 1100 volts
- Millivolt/Ohms option on one board
- External Reference for bipolar ratio measurement
- Fully isolated remote programming
- Fully isolated data (printer/computer) output
- AC/AC ratio
- Add options any time on order or in the field for the same cost

SPECIFICATIONS

Ranges:	10V, 100V, 1000V
Accuracy:	±(0.005% of reading + 0.001% of range) 24 hours; 23°C ±1°C ±(0.01% of reading + 0.003% of range) 90 days
Input Impedance:	> 10^{10} ohms at all times on 10V range 10^{7} ohms on 100V and 1000V ranges
Normal Mode Rejection Ratio:	> 60 db, 50 Hz and up
Common Mode Rejection Ratio:	140 db DC to 60 Hz (filtered) with 1K unbalance to low terminal
Speed:	25 ms max unfiltered 500 ms max unfiltered
Max Auto Range:	80 ms unfiltered

GENERAL

Variable Sample Rate:	Local: Variable 10/sec to 1 per 3 sec External: 40/sec maximum
Maximum Conversion Time:	25 ms, after sample pulse
Warmup:	30 minutes
Operating Temperature:	0°C to 50°C
Power:	115/230 VAC±10% at 50 to 440 Hz 20 watts with all options
Size:	3½" high x 17½" wide x 15" deep
Weight:	12 to 15 lbs.
Price (8300A):	$1295

OPTIONS—Refer to page 4

8300A OPTIONS

AC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy: (90 days)	±(0.1% of reading + 0.005% of range) 50 Hz to 20 kHz. Total freq. response, 30 Hz to 100 kHz
Input Impedance:	1 megohm < 100 pf
Speed:	500 ms to within 0.1% of final reading
Price: (—01 option)	$450.00

EXTERNAL REFERENCE (RATIO)

Reference Range	+2V to +10.5V
Accuracy:	$\pm(0.01\% \text{ of reading} + \frac{0.003\% \times 10V}{V_{ref}} \text{ of range})$
Input Resistance:	1 megohm
Speed:	500 ms to ±0.01% of final reading
Isolation:	True 4-terminal ratio capability. Up to ±12V commons separation
Normal Mode Rejection Ratio:	> 30 db at 60 Hz.
Price: (—05 option)	$200.00 (requires —07 rear term. acc. $25.00)

DATA OUTPUT (Fully Isolated)

Data Available:	Function, Range, Polarity and Digits.
Flags:	Ready, Overload.
Controls:	External Trigger, Fast/Normal Data Transfer
Logic Levels	+5V thru 6K—1, OV=0 (Series 930 DTL)
Price: (—03 option)	$500.00

REMOTE CONTROL (Fully Isolated)

Input Definition:	Series 930 DTL
Control Modes:	DTL, TTL or contact closure
Logic Levels:	+5V; no command 0V or switch closure; call up function
Price: (—04 option)	$200.00

* MV/Ohms and AC/AC ratio options cannot simultaneously be installed in an 8300A. The 8300A will accept either option at any time, however.

MILLIVOLT/OHMS*

Resistance Ranges:	1K, 10K, 100K, 1000K, 10M
Accuracy: (90 days)	1K thru 100K: ±(0.01% of reading + 0.003% of range) 1000K: ±(0.02% of reading + 0.003% of range) 10M: ±(0.05% of reading + 0.003% of range)
Measurement Voltage:	1.1V for 1K and 10K at full range 10V for 100K to 10M at full range 0 at short circuit input
Speed:	Within 0.01% of final reading in 75 ms 100K thru 10M and 1 sec 1 K and 10K
Millivolt Ranges:	100 mv, 1000 mv
Accuracy: (90 days)	100 mv: ±(0.01% reading + 0.01% full scale) 1000 mv: ±(0.01% reading + 0.003% full scale)
Input Impedance:	1000 mv: = 1000 MΩ, 100 MV = 100 MΩ
Speed:	100 mv: 3 sec to within 0.01% of final reading 1000 mv: 1 sec to within 0.01% of final reading
Normal Mode Rejection Ratio:	>60 db, 50 Hz and up
Common Mode Rejection Ratio:	>140 db DC to 60 Hz
Overload:	1100V DC without damage
Price: (—02 option)	$350.00

AC/AC RATIO *

Reference Voltage Range:	0.2V to 105V in three ranges.
Input Impedance:	1 megohm shunted by < 100 pf
Ratio Accuracy:	$\pm(0.05\% \text{ of input } \frac{\pm 0.005\% \times \text{Ratio Range}}{E_{Ref}}$ % of range) 50 Hz –20 kHz.
Price: (—08 option)	$700 (Note: Options —01, —05, and —07 must be installed to use AC/AC Ratio option)

NEW-NEW-NEW

PROGRAMMABLE VOLTAGE/ CURRENT CALIBRATOR– MODEL 3330A

The Model 3330A is a fully programmable constant voltage/constant current Calibrator. This Calibrator provides output voltages from 0-1000V in 3 ranges and constant current outputs from 0-100 ma in three ranges, with 11% overranging on each range. Voltage accuracy is ±0.005%. Constant current accuracy is ±0.01%.

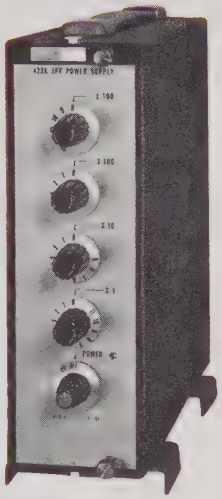
BRIEF SPECIFICATIONS

MODE	VOLTAGE RANGE	MAX. CURRENT	CURRENT RANGE	COMPLIANCE VOLTAGE	ACCURACY	REGULATION LINE-LOAD	STABILITY PPM OF OUTPUT	PRICE
CONSTANT VOLTAGE	10, 100, 1000V	100 ma 50 ma			±0.005%	5 ppm of output	25 ppm Per mo.	$2995.00
CONSTANT CURRENT			1, 10, 100 ma	1000V 500V	±0.01%	5 ppm of range	50 ppm Per mo.	

NEW-NEW-NEW

NIMS HIGH VOLTAGE POWER SUPPLY-MODEL 423A

Designed for Nuclear Instrument Module Systems (NIMS), The Model 423A is a versatile high voltage power source in a small package. Contained in either a portable bench case or a NIMS bin, the Model 423A features remote analog slewing of the output, or manual operation in steps of 10, 100 and 500 volts. A Sweep Vernier allows control of the output from zero to the calibrated dial settings.



BRIEF SPECIFICATIONS

OUTPUT VOLTAGE	OUTPUT CURRENT	ACCURACY	RESOLUTION	SLEWING	RIPPLE & NOISE	OVERLOAD PROTECTION	POLARITY
0 to ± 3000 VDC	0-10 ma	0.25% or 1.25V whichever is greater	100 mv	0 to dial setting with vernier	5 mv p-p	Output limited to 15 ma	Reversible at rear panel

SIZE 3 inches by 9 inches by 10 inches

VOLTAGE CALIBRATION

0 to 2500 V in 5 steps of 500V
0 to 400V in 4 steps of 100V
0 to 90V in 9 steps of 10V
0 to 10V vernier

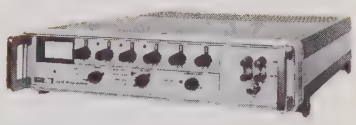
PRICE

Basic Unit	$460.00
Carrying Case	$35.00
△ E Option	$50.00

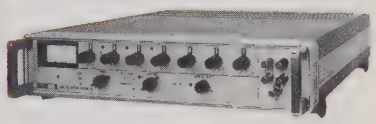
NEW-NEW-NEW

DC VOLTAGE CALIBRATOR– MODELS 341A AND 343A

The Fluke Models 341A and 343A DC Voltage Calibrator are outstanding new additions to the Fluke line of all solid-state ultra-precise and stable DC Calibrators. Both instruments cover 0-1111 volts dc in three ranges of 10, 100, and 1000 volts, each with 11% overranging. For the Model 341A, calibration accuracy is an absolute ±0.01% of setting from 0.3 volt to 1111 volts. Calibration accuracy for the Model 343A is ±0.003% of setting from 0.7 volt to 1111 volts. Each Model has current limiting crowbar protection and a four-terminal floating output.



Model 341A



Model 343A

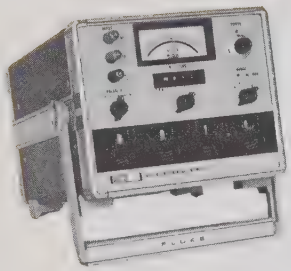
BRIEF SPECIFICATIONS

MODEL	OUTPUT VOLTAGE	CURRENT OUTPUT	ACCURACY	REGULATION LINE-LOAD	STABILITY % PER MO.	RIPPLE (rms)	RESOLUTION PPM OF RANGE	PRICE
341A	0 to 1111.110V	25 ma	±0.01% (6 mos.)	0.0005%	±0.003%	<100 uv	1 ppm	$1195.00
343A	0 to 1111.1110V	25 ma	±0.003%	0.0005%	±0.0015%	<50 uv	0.1 ppm	$1795.00

VOLTMETERS

Fluke AC/DC and DC Differential Voltmeters offer the widest range of performance and accuracy in the market. Most units operate from either internal rechargeable batteries or 115/230V, 50-440 Hz line power. Battery power is essential for measurement where maximum accuracy demands complete line isolation. Input ranges are 1, 10, 100 and 1000V each with 10% overranging. Fluke Differential Voltmeters are electrically and mechanically designed to perform under the extremes of temperature, shock, vibration and humidity. The internal reference voltage is developed from matched zener diodes that are selected to establish excellent stability, tracking and temperature coefficient parameters. Fluke manufactures all of the precision wire-wound resistors used in these instruments. The all solid-state differential voltmeters are lightweight for portability and are provided with a tilt-back bail, or functional detented handle for operator convenience. Recorder output feature is available on all Fluke Differential Voltmeters.

DIFFERENTIAL VOLTMETERS



Model 891A

Model 883A

Model 881A

Solid State DC

MODEL	INPUT	DIFF. ACCURACY % OF INPUT	POWER	PRICE
881A	0-1100 VDC	±0.005%	115 or 230 VAC	881A – $895.00 881AB – $995.00
885A	0-1100 VDC	±0.0025%	115 or 230 VAC	885A – $1060.00 885AB – $1160.00
891A & AR	0-1100 VDC	±0.01%	115 or 230 VAC	891A & AR – $745.00 891A-01 – $845.00
895A	0-1100 VDC	±0.0025%	115 or 230 VAC	895A – $1250.00
896A	0-15 kv	±0.005% ±0.1% from 1 kv to 15 kv	115 or 230 VAC	896A – $1995.00

Solid State AC/DC

MODEL	INPUT	DC ACCURACY % OF INPUT	AC ACCURACY %	FREQUENCY RANGE	POWER	PRICE
883A	0-1100V	±0.005%	±0.1%	20 Hz to 5 kHz from 1 mv to 1100V	115 or 230 VAC	883A – $1295.00 883AB – $1395.00
887A	0-1100V	±0.0025%	±0.1%	20 Hz to 5 kHz from 1 mv to 1100V	115 or 230 VAC	887A – $1495.00 887AB – $1595 00
893A & AR	0-1100V	±0.01%	±0.15%	20 Hz to 20 kHz from 1 mv to 1100V	115 or 230 VAC	893A & AR – $1045.00 893A-01 – $1145.00

RACK MOUNTING CONFIGURATIONS

Kits are available for side-by-side, center or left/right side rack mounting of most half rack width Fluke Voltmeters. Kits are also available for mounting full rack width voltmeters and calibrators.

TRUE RMS DIGITAL VOLTMETER–MODEL 9500A

The 9500A precisely measures the true RMS value of any AC signal up to 1100 volts RMS regardless of waveshape or harmonic content. Input range selection, decimal point, and calibration are truly automatic. Nixie® tubes provide a digital display, readable over a wide viewing angle. Both display and range may be varied by means of front panel control.

VOLTAGE RANGE: 1 mv to 1100V RMS

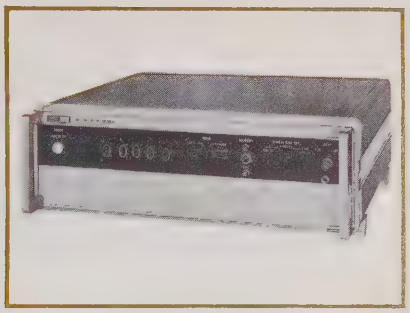
ACCURACY: ±(0.05% of input + 0.015% of range) from 50 Hz to 10 kHz
Reduced accuracy specifications from 20 Hz to 700 kHz

FREQUENCY: 20 Hz to 700 kHz

INPUT RESISTANCE: 1 megohm shunted by 17 pf

INPUT POWER: 115/230 VAC, 50-440 Hz

PRICE: $2485.00



TRUE RMS DIFFERENTIAL VOLTMETER–MODEL 931B

The Model 931B combines the advantages of a true RMS voltmeter for accurate measurement without waveform error and the null balance accuracy of a differential voltmeter.

VOLTAGE RANGE:
Differential Mode: 0.01 to 1100V RMS in 5 ranges (10% overranging)
Direct Mode: 0.003 to 1100V RMS in 11 ranges

CREST FACTOR: Differential Mode: 10

INPUT POWER: 115/230V AC, 50 – 440 Hz

ACCURACY:
Differential Mode: ±(0.05% of reading +0.005% of range) from 30 Hz to 50 kHz. Reduced accuracy specifications from 2 Hz to 1 MHz
Direct Mode: ±3% of end scale

INPUT IMPEDANCE: 1 megohm shunted by less than 8 pf

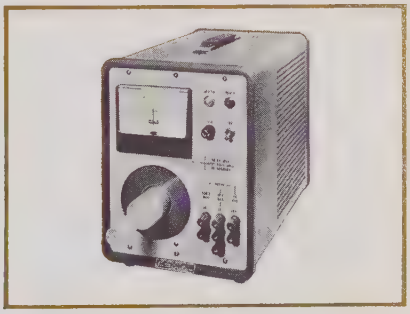
PRICES: $995.00

PRECISION VOLTAGE DIVIDERS–MODELS 80D AND 80E

The Models 80D and 80E are tapped for 10 and 1V outputs at rated input, for use with all Fluke differential voltmeters and any conventional potentiometer.

MODEL NO.	MAX. INPUT VOLTAGE	TOTAL RESISTANCE	DIVISION RATIO 500V OUT	DIVISION RATIO 10V OUT	DIVISION RATIO 1V OUT	DIVISION RATIO ACCURACY	PRICE
80E-5	5 kv	5 Meg	–	500:1	5,000:1	±0.01%	$ 350.00
80E-10	10 kv	10 Meg	–	1000:1	10,000:1	±0.01%	$ 395.00
80D-30	30 kv*	30 Meg	60:1	3000:1	30,000:1	±0.01%	$1,195.00

*Intermediate voltages between 10 KV and 30 KV available upon request.



DIFFERENTIAL MULTIMETER-MODEL 853A

The Model 853A is an all solid-state, extremely accurate low cost multimeter utilizing differential techniques to measure AC/DC voltages and current and resistance. The instrument may be operated from line and/or rechargeable or replaceable batteries.

ACCURACY: ±(0.2% + 0.02% FS) for DC voltage and current
±(0.5% + 0.05% FS) for AC voltage and current

VOLTAGE RANGE: 0 – 1100 VAC/DC in 4 ranges

FREQUENCY RANGE: 20 Hz to 30 kHz

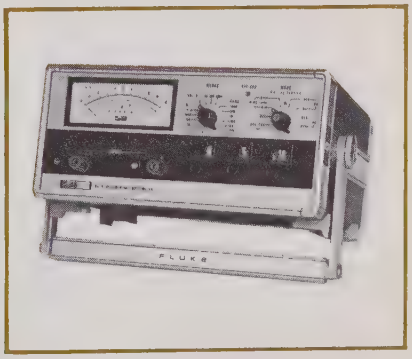
CURRENT RANGE: 0 – 10 amps AC/DC in 6 ranges

RESISTANCE RANGE: 0 – 100 megohms in 7 ranges

ACCURACY: ±(0.2% + 0.01% FS)

OVERLOAD PROTECTION: 1200V RMS or DC on any range. 12 amps on 10 amp range. 2 amps on all other ranges

PRICE: $545.00 Replaceable Battery
$595.00 Rechargeable Battery



TRANSIT CASES

Where operation and storage in severe relative humidity conditions (up to and including 100%) are required, most Differentials are available with splash-proof panel and MIL-T-945A combination case.

VOLTAGE AND CURRENT CALIBRATORS

Model 335A

Model 382A

The Fluke line of voltage and current calibrators combine ruggedness and reliability with extreme accuracy, and stability. Most units are provided with current and voltage limit functions. All solid-state models are equipped with zener diode reference elements, housed in proportionately controlled temperature ovens.

MODEL	VOLTAGE	CURRENT	REGULATION LINE	REGULATION LOAD	STABILITY, % HOUR	STABILITY, % DAY	STABILITY, % PER MO.	CALIBRATION ACCURACY	MAX. RIPPLE RMS	PRICE
313A	0-50	0-2A	0.0005	0.0005	0.002	0.0025	0.005	0.01%	50 uv	$1395.00
332B	0-1111	0-50 ma	0.0002	0.0002		0.002 /year		0.002%	20-40 uv	$2445.00
335A*	0-1111	0-50 ma	0.0002	0.0002		0.002 /year		0.002%	20-40 uv	$2645.00
	(Model 335A is also a 20 ppm differential voltmeter and nine range, high input impedence galvanometer)									
382A**	0-50	0-2A	0.0005	0.0005	0.002	0.0025	0.005	0.01%	50 uv	$1595.00
382A†	0-50	0-2A (4 ranges)	0.0005	0.001	0.0025		0.005	0.02%	0.002% of range	

*Calibrator Portion Only.
**Voltage Mode.
†Current Mode.

METER CALIBRATOR–MODEL 760A

The Model 760A Meter Calibrator is a complete all solid-state calibration system for AC and DC voltmeters, ammeters, ohmeters, and multimeters. Interlocks and safety features are provided to protect both the operator and the instrument being calibrated.

	DC VOLTAGE AND CURRENT	AC VOLTAGE AND CURRENT
VOLTAGE RANGE:	0.001V to 1000V in 0.1 mv steps	0.001V to 1000V in 0.1 mv steps
VOLTAGE ACCURACY:	±(0.1% of setting + 25 uv) Also ±0.33% at 1 mv, 3 mv, and 10 mv	±(0.25% of setting + 25 uv) Also ±0.33% at 1 mv, 3 mv, and 10 mv
CURRENT RANGE:	1 ua to 10A in 1 ua steps	1 ua to 10A in 1 ua steps
CURRENT ACCURACY:	±(0.25% of setting + 0.025 ua)	±(0.25% of setting +0.025 ua)
FREQUENCY:		60 Hz and 400 Hz (60 Hz phase locked to power line)
RESISTANCE:		
Range:	0 to 10 megohms	
Accuracy:	±(0.1% of setting + 0.5 ohm)	
Resolution:	1 ohm	
PRICE:	$2845.00	

NULL DETECTOR MICROVOLTMETER–MODEL 845AB

The Models 845AB and 845AR are designed for extremely high input resistance, sensitivity and isolation. Typical applications are standardization of voltage dividers and true comparison of standard cells, ratio measurements and many more.

INPUT RANGES: 1 uv to 1000 VDC in 19 end-scale ranges

ACCURACY: ±(2% end scale + 0.1 uv)

INPUT RESISTANCE: 100 megohms on 300 mv range and above
10 megohms on 100 mv range and below

INPUT POWER: 845AB rechargeable battery or 115/230 VAC ±10%, 50-440 Hz
845AR 115/230 VAC ±10%, 50-440 Hz

PRICE: $435.00

HIGH VOLTAGE POWER SUPPLIES

Fluke high voltage power supplies have become the standard of the industry where quality and reliability are essential. They provide unexcelled performance through sound electrical and mechanical design. Voltages from 0-10,000 and from10,000 to 30,000 are available with current capabilities from 0-50 ma. All instruments incorporate over-current protection circuits.

MODEL	VOLTAGE	CURRENT (ma)	REGULATION LINE	REGULATION LOAD	STABILITY (%) PER HR.	STABILITY (%) PER DAY	CALIBRATION ACCURACY (% of Output)	MAX. RIPPLE RMS	RESOLUTION	PRICE
412B	0-2100V	0-30	0.001	0.001	0.005	0.02	0.25	500 uv	5 mv	$ 410.00
415B	0-3111V	0-30	0.0005	0.0005	0.002	0.01	0.25	100 uv	5 mv	$ 575.00
408B	0-6000V	0-20	0.001	0.001	0.005	0.02	0.25	1 mv	5 mv	$ 700.00
410B	0-10, 000V	0-10	0.001	0.001	0.005	0.02	0.25	1 mv	5 mv	$ 975.00
430A	10KV-30.22KV	0-10	0.005	0.01	0.005	0.03	0.25	5 mv	100 mv	$3940.00

GENERAL PURPOSE POWER SUPPLY- MODEL 407D

VOLTAGE:
0-555V

REGULATION:
Line – 0.005%
Load – 0.01%

CURRENT:
0-300 ma

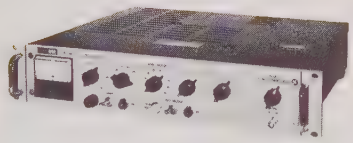
STABILITY:
Per hour – 0.01%
Per day – 0.05%

CALIBRATION ACCURACY:
0.5%

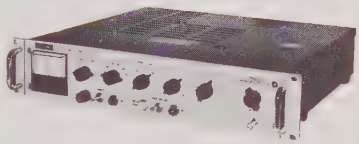
MAX. RIPPLE RMS:
500 uv

RESOLUTION:
2 mv

PRICE:
Cabinet Model (407D) – $450.00
Rack Model (407DR) – $470.00



Model 415B



Model 412B

RATIO MEASUREMENT DEVICES

Fluke provides Kelvin-Varley dividers, reference dividers and lead compensators for use in calibration consoles and ratio measuring systems. Each unit meets the most exacting requirements of the standards laboratory.

KELVIN-VARLEY DIVIDERS

MODEL	INPUT RESISTANCE	LINEARITY	RESOLUTION	MAX. INPUT	VOLTAGE MAX. PWR.	TC OF LINEARITY	PRICE
720A	100k ohm ±0.005% at 1.0 input 110k ohm ±0.005% at 1.1 input	±.1 ppm at dial setting of 0.1 to 1.1	0.1 ppm	1100V	11 watts	±0.1 ppm of input/°C	$1495.00
725A	440k ohm ±0.2% at 1.1 input	±5 ppm at dial setting of 0.1 to 1.1	1 ppm	1100V	2.7 watts	±1 ppm/°C	$ 390.00

REFERENCE VOLTAGE DIVIDER–MODEL 750A

INPUT VOLTAGES	OUTPUT VOLTAGES	DIVIDER CURRENT	TC OF OUTPUT	ACCURACY	STABILITY	PRICE
1.1, 5, 10, 50, 100, 500, 1000, 1100V DC	0.1, 0.5, 1, 1.1, 5, 10, 50, 100, 500, 1000, 1100V DC	1 ma	±1 ppm/°C over operating range	±0.001%	±0.001% per year	$1195.00

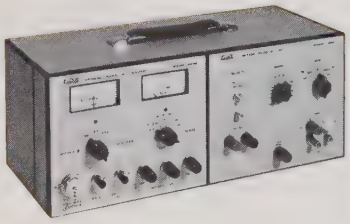
LEAD COMPENSATOR–MODEL 721A

4000:1 Max. Ratio Resistance, 0.1 milliohms resolution, 1500 Max. Divider Voltage, Price $295.00

DC CALIBRATION SYSTEMS

The 7100 series DC voltage and ratio calibration systems offer the utmost in accuracy and flexibility. Many combinations and variations are possible, all utilizing off-the-shelf standard Fluke instruments. The 7100 systems may be completely tailored to your individual calibration and measurement applications. Typical applications are calibration of differential voltmeters, digital voltmeters, voltage dividers, reference power supplies, laboratory potentiometers and many more.

THERMAL TRANSFER STANDARD–MODEL 540B



For ±0.01% RMS AC transfer measurements without calibration curves or correction tables, Fluke offers the all solid-state Model 540B AC/DC Thermal Transfer Standard. Thermocouple burnout is virtually eliminated by a unique protection circuit. In addition a search circuit provides visual indication of the percent of rated input. DC input to the unit is conveniently reversed via front panel switch, and DC turnover is held to less than 0.01%.

VOLTAGE RANGE: 0.5 to 1000V in 14 ranges
GALVANOMETER RESOLUTION: 0.0012% of input/scale div. at rated input
ACCURACY (% OF INPUT)

RANGE	FREQUENCY	AC/DC DIFFERENCE
All except 1000V	5 Hz-50 kHz	±0.01%
1000V	5 Hz-20 kHz	±0.02%
1000V	20 kHz-50 kHz	±0.04%
0.5 thru 10V	50 kHz-1 MHz	±0.1%

PRICE: $1045.00 (RECHARGEABLE BATTERIES INCLUDED)

CURRENT TRANSFER ACCESSORIES

Available as accessories for the Model 540B are Thermal Converters (A55), Current Shunts (A40), a Current Transfer Switch (A45), Coaxial Cable Kits (A55-110), and Storage Cases (C41 and C55). See your local representative or contact the John Fluke Mfg. Co., Inc. for more information.

ELECTRONIC GALVANOMETER–MODEL 841A

Unique design, features fast response, virtual immunity to overload damage, battery or AC operation and operation in any position.

FULL SCALE RANGES:

841A
±30 nanoamperes (2 na/scale div.)
±300 nanoamperes (20 na/scale div.)
±3 microamperes (200 na/scale div.)

841B
±100 nanoamperes (5 na/scale div.)
±1 microampere (50 na/scale div.)
±10 microamperes (500 na/scale div.)

INPUT RESISTANCE:
841A—180 ohms
841B—18 ohms

PRICE: $295.00

TIME AND FREQUENCY

FREQUENCY SYNTHESIZER–MODEL 644 SERIES

The all solid state 644 Series Frequency Synthesizers cover the frequency range of 0 to 40 MHz with 3 instruments. The Model 644 provides DC to 40 MHz; the 633 from DC to 11 MHz and the 622 from DC to 2 MHz. All instruments are of modular construction and have the same characteristics of 90 db spectral purity, low phase noise and low noise floor. In addition, all have sweep and search capabilities and can be remotely programmed.

MODEL	FREQUENCY RANGE	FREQUENCY INCREMENTS	FREQUENCY STABILITY AND ACCURACY	PRICE
644A	DC to 40 MHz	0.1 Hz	1 part in 10^8 per day	$10,990.00
633A	DC to 11 MHz	0.1 Hz	1 part in 10^8 per day	$ 7,790.00
622A	DC to 2 MHz	0.1 Hz	1 part in 10^8 per day	$ 7,190.00

NEW-NEW-NEW

FREQUENCY SYNTHESIZER–MODEL 645A

The new Fluke Model 645A Frequency Synthesizer covers the frequency range from DC to 50 MHz in .01 Hz step increments. The spectral purity of this new instrument is at an all time high. All non-harmonically related spurious signals are at least 100 db below the fundamental. The signal-to-phase-noise ratio is also greatly improved. The 645A contains all of the versatile features of the 600 Series family such as, high speed remote programming, internal sweep generator, and modular construction suitable for many varieties of special versions. In addition, the variety of standard options allows tailoring the 645A to most applications, at a bare minimum cost to the customer. The 645A embodies all of the latest state-of-the-art improvements in synthesizer design and packaging to achieve a new standard of performance.

FREQUENCY RANGE	FREQUENCY INCREMENTS	SPURIOUS	FREQUENCY STABILITY AND ACCURACY	SIGNAL-TO-PHASE NOISE RATIO	PRICE
DC to 50 MHz	.01 Hz	All non-harmonically related spurious signals are at least 100 db below the fundamental	1 part in 10^8 per day	Greater than 63 db in a 30 Hz band centered on the carrier but excluding a 1 Hz band centered on the carrier	$13,500.00

FREQUENCY COMPARATOR–MODEL 103A

The Model 103A now makes possible the comparison of test and reference frequencies from 100 kHz to 1 MHz in 100 kHz steps and from 1 MHz to 5 MHz in 1 MHz steps. Output may be read directly on external frequency counter, front panel meters and/or output recorder. Quadrature outputs are available for display on an oscilloscope or XY recorder. Price $1995.00.

FREQUENCY DISTRIBUTION AMPLIFIER-MODEL 203A

The Model 203A is a multi-channel distribution amplifier that features high stability, free from harmonics and spurious outputs and high inter-channel isolation. These amplifiers are being widely used for distribution of standard frequencies in laboratories, communication installations and industrial facilities. Price $1395.00.

VLF RECEIVER/COMPARATOR–MODEL 207-1

The Model 207-1 is a coherent VLF tracking receiver for calibration of laboratory and communications center frequency standards. Frequency coverage is from 8.0 to 31.9 kHz in steps of 100 Hz with an additional channel at 60 kHz. The instrument is all solid-state and employs a multitude of integrated circuits. Multi-channel capability plus high sensitivity assures round-the-world reception of VLF signals for frequency standardization. Price $2995.00.

OMEGA COMMUTATOR–MODEL 291A

The Omega System of global navigation utilizes a network of highly stable transmitters operating in the VLF spectrum. The Model 291A Omega Commutator is designed to permit selected use of these ultra-stable transmissions for frequency comparison in the 207 series VLF Receiver/Comparators. Price $495.00.

VAW® METER–MODEL 102

The Model 102 Vaw® Meter measures voltage, current, and power over a wide frequency range. It has a maximum true power sensitivity of 225 microwatts and will measure up to 18 kilowatts over the frequency range of 20 Hz to 100 kHz. Cabinet model, $760.00, shunts $30.00 each.

GENERAL INFORMATION

Of necessity information and specifications contained in this brochure are abbreviated. Detailed technical data sheets will be furnished immediately upon request from the Fluke engineering representative in your area, or directly from the factory.

Orders should be made out to John Fluke Mfg. Co., Inc., sent in care of your local Fluke representative or directly to P.O. Box 7428, Seattle, Washington 98133.

U.S. and Canadian terms are 30 days net.

Prices are F.O.B. factory, Mountlake Terrace, Washington, unless otherwise specified. All prices are U.S. funds and are subject to change without notice.

All Fluke instruments are warranted against defective materials and workmanship for one year. All power transformers are warranted for the life of the instrument. Tubes and lamps are considered expendable components and are warranted for 90 days.

* * * * * *

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FLUKE

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Bud Lord · Filaka
Madge Dunbar · SBM

JOHN FLUKE MFG. CO., INC. ■ MODEL **8100A**

FLUKE

DIGITAL MULTIMETER

FEATURES:

- *"RECIRCULATING REMAINDER" * A/D CONVERSION*
- *INTERNAL BATTERY OPERATION OPTIONAL*
- *COMPLETE MULTIMETER*
- *FOUR DIGITS PLUS OVERRANGE*

APPLICATIONS:

- *MEASURE AC AND DC TO 1200 VOLTS*
- *MEASURE RESISTANCE TO 12 MEGOHMS*
- *COMPLETE PORTABILITY WITH BATTERY OPTION*
- *FULLY ISOLATED MEASUREMENTS*

* Patent Pending

DESCRIPTION

Model 8100A is a compact, lightweight digital multimeter displaying four full decades plus a "1" for 20% overrange. It may be operated from line power or optional self-contained rechargeable batteries. AC volts, DC volts and kilohms are standard functions, selection being made via pushbutton switches. A switched 2-pole active filter and instantaneous, automatic polarity selection and display are additional standard features.

Analog inputs to the 8100A are processed through a buffer amplifier, the output of which is periodically sampled by a unique, Fluke designed, "Recirculating Remainder" analog-to-digital converter. The converter uses only one BCD counter and resistive ladder network to serially determine and display all digits. A unique capacitor register is used to hold the digits of the sample for continuous display between samples. Necessary converter switching is accomplished with field-effect transistors.

The analog circuitry also makes multiple use of scaling resistors and passive components. The combined analog and digital circuitry has low power consumption and a low total parts count, which leads to high reliability and optional battery operation.

High quality wire-wound resistors, polystyrene capacitors and an extremely stable reference amplifier are used in conjunction with the buffer amplifier and a high accuracy comparator to ensure precise, stable, digitizing of the analog input.

Custom packaging of the 8100A combines an attractive appearance with rugged construction. A single fiberglass circuit board is solidly secured to its strong aluminum chassis. Guard shields surround all critical analog and digital circuitry. Tough, scuff resistant plastic covers provide exterior protection. An accessory cover is available to protect the front panel during transit. A locking tilt-up bail is also used as a carrying handle. The line cord is detachable. A concealed slide switch at the rear of the instrument is used for selection of 115V or 230V AC line power.

The optional, rechargeable battery pack may be installed in the field or factory. A meter along side the digit readout is provided to indicate the state of battery charge. The battery is automatically charged when the 8100A is operated from line power. Disconnecting the line cord enables battery operation.

SPECIFICATIONS

DC VOLTS

Ranges	±1V, ±10V, ±100V and ±1000V 20% overrange on all ranges.
Resolution	0.01% of range. (100 uv on 1V range maximum)
Accuracy	
30 days, 20°C to 30°C	±(0.02% of input + 0.01% of range)
90 days, 15°C to 35°C	±(0.05% of input + 0.01% or range)
DC Input Resistance	Constant 10 megohms on all ranges.
Filter	Switch selected 2-pole, linear phase active filter.
Response Time to Rated Accuracy (max.)	0.5 seconds with filter out. 1.5 seconds with filter in.

SPECIFICATIONS *(Continued)*

Rejection . . . . . .

		INTERFERENCE FREQUENCY			
		60 Hz		50 Hz	
	DC	FILTER IN	FILTER OUT	FILTER IN	FILTER OUT
COMMON MODE (1K in Low Lead)	120 db	120 db	100 db	120 db	100 db
NORMAL MODE	----	60 db	20 db	47 db	9 db

NOTE: Common Mode Rejection approaches infinity when instrument is battery operated.

Polarity . . . . . Automatic, instantaneous selection and display.

Overload . . . . . ±1200 VDC or ±1700V peak AC can be applied continuously to any range without damage.

AC VOLTS

Ranges . . . . . 1V, 10V, 100V and 1000V. 20% overrange on all ranges.

Resolution . . . . . 0.01% of range. (100 uv on 1V range maximum)

Accuracy . . . . . MIDBAND 50 Hz - 10 kHz / EXTENDED 30 - 50 Hz and 10 - 20 kHz

90 days, 15°C to 35°C: ±(0.2% of input + 0.05% of range) / ±(0.5% of input + 0.1% of range)

Input Impedance . . . . . 1 megohm shunted by < 30 pf.

Response Time to Rated Accuracy . . . . . 3 seconds.

Maximum DC Normal Mode Voltage . . . . . ±1200 VDC NOTE: The sum of DC Normal Mode Voltage and peak AC voltage must not exceed ±1700V.

Overload . . . . . ±1200 VDC or ±1700V peak AC from 30 Hz to 20 kHz can be applied continuously to any range without damage.

RESISTANCE

Ranges . . . . . 1K, 10K, 100K, 1000K and 10M. (20% overrange on all ranges)

Resolution . . . . . 0.01% of range (0.1 ohm on 1K range maximum)

Accuracy . . . . . 1K - 1000K / 10M

30 days, 20°C to 30°C: ±(0.05% of input + 0.01% of range) / ±(0.1% of input + 0.01% of range)

90 days, 15°C to 35°C: ±(0.1% of input + 0.02% of range) on all ranges

Configuration . . . . . Two terminal, constant current.

Voltage Across Input . . . . . 1.0V at full range.
1.2V at 20% overrange.
9V with open terminals.

Power In Unknown R . . . . . ⩽ 1 milliwatt in range and ⩽ 1.44 milliwatts at 20% overrange on the 1K range, decreasing by an order of magnitude per range to 100 nanowatts at 10 megohms.

Response Time to Rated Accuracy	1K - 1000K	10M
Filter Out	0.5 seconds	3.0 seconds
Filter In	2.0 seconds	10.0 seconds

Overload

1K Range . . . . . 130V RMS may be applied continuously without damage.

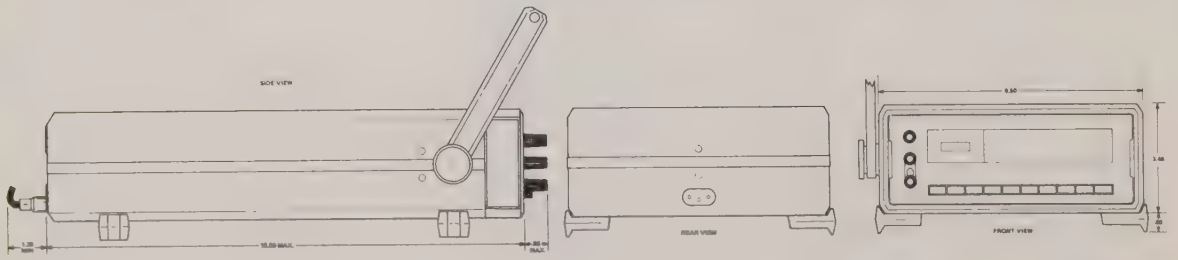
1K - 10M . . . . . 230V RMS may be applied continuously without damage.

SPECIFICATIONS *(Continued)*

GENERAL

Selection	Manual via mechanically interlocked pushbuttons.
Display	Four decade neon in-line readout with polarity neon for DC volts and fifth digit for 20% overrange. Automatic decimal location.
Sample Rate	3 samples per second.
Maximum Inputs	
"HI" to "LO"	See "Overload" specification by function.
"LO" to "Guard"	100V DC or peak AC.
"Guard" to "Chassis"	1200V DC or 230V RMS at 60 Hz.
Power	8 watts from 115V/230V, ±10%, 50-500 Hz line with internal battery option –01. 8 hours continuous operation from the rechargeable nickel-cadmium batteries.
Weight	8 pounds without batteries. 10 pounds with batteries.
Storage Temperature	–40°C to +75°C. (–40°C to +60°C with batteries)
Operating Temperature	0°C to +50°C.
Temperature Coefficient (outside limits shown in 30 and 90 day specifications)	DC ±(0.0025% of input +0.001% of range)/°C AC ±(0.015% of input +0.005% of range)/°C KΩ ±(0.0035% of input +0.0015% of range)/°C 10 MΩ ±(0.01% of input +0.002% of range)/°C
Humidity Range	80% R.H. max. at temp. ⩽ 35°C; 70% R.H. max from 35°C to 50°C.
Shock and Vibration	Meets requirements of MIL-T-21200G and MIL-E-16400F.
Mounting	Tilt down carrying handle detents into custom non-marring feet and serves as a tilt-up bail for bench use.

Price:	Model 8100A	$695 (without battery)
	Model 8100A-01	$795 (factory installed battery option)
	8100A-01 Kit	$100 (for field installation of battery option)
Accessories:	80-RF	$100 (R.F. Probe, 500 MHz)
	80F-5	$150 (High Voltage Probe, 5 kv)
	80F-15	$175 (High Voltage Probe, 15 kv)
	A-90	$255 (6 Range AC/DC Current Shunt to 10A)
	MEE-4008	$10.00 (Front Panel Dust Cover)
	MEE-7006	$40.00 (Rack Mtg. Ears -- Single Unit, Center Mount)
	MEE-7013	$40.00 (Rack Mtg. Ears -- Single Unit, Right or Left Offset)
	MEE-7014	$25.00 (Rack Mtg. Kit -- Two Units , Side-by-Side)



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8100A DIGITAL MULTIMETER OPERATIONAL THEORY

The 8100A consists of three main sections, referring to Figure 1 and the Schematic Drawings.

1. The Buffer section acts as a signal conditioner, capable of dividing voltage inputs, filtering and impedance conversion. The input divider also functions as a portion of the current source in the resistance ranges. (See Figure 2)
2. The Analog/Digital Conversion system, accepts the output from the Buffer and digitizes it using FLUKE'S Recirculating Remainder system of conversion. The unit samples three times a minute and recycles every 20 milliseconds.
3. The display section accepts the BCD output of the Analog to Digital Converter and puts it into ten line decimal output and displays the result on NIXIE tubes on a timed pulse basis.

In addition to the three main sections described above, the Power Supply serves dual functions. In addition to supplying the voltages required by the instrument it also contains an inverter that is used to both produce operating voltages for the instrument and supplies the clock or synchronization for timing the instrument.

Power for the 8100A is supplied by either the AC power line or via the internal battery pack, as furnished with the -01 option. When operated from line voltage transformer T101 provides two outputs. One output is rectified and filtered and used for the −18 volt supply in the instrument. The other winding provides a higher voltage which is rectified and used to charge the battery option, through DS11 which acts as a series limiting element.

The voltage supplied by the line voltage conversion is always greater than the voltage from the batteries, back biasing CR34 which prevents draining the batteries. The negative voltage, from either the batteries or the rectifiers CR1 and CR2, is regulated and filtered after passing through the protective fuse F2 and then on to supply the instrument all of it's negative voltage needs.

The −18 volts operates a 250 Hz inverter consisting of Q4, Q5 and a driver transformer T102. The output voltages from T102 are then conditioned to supply the remaining potential needs of the 8100A.

A high voltage winding (100v) operates a doubler rectifier circuit which provides 200v DC which is pulsed on every 4 milliseconds for 2 milliseconds. This provides a pulse for the last half of each time period of the instrument. This +200v DC is used to pulse the readout tubes.

T102 also provides one output which is rectified and filtered to +5 volts which is used to supply all of the integrated circuit logic. Another winding of T102 provides a voltage which is rectified and regulated to provide the +15 volts needed as a positive supply in the instrument. This +15 volts is further dropped by a zener regulated circuit to provide the +7.0 volt reference needed in the 8100A. This +7.0 volt reference supply has a fixed load of 2 ma in R181 and is protected from current reversals when an overload occurs in the ohms configuration by CR10.

INPUT RANGE DIVIDER (Figure 2)

The function switching on the front panel will provide one of the four basic configurations shown in Figure 2. When the instrument is operated in the DC volts position the divider will provide divisions of 1, 10, 100 and 1000 in order to maintain a 1 volt in put into the Buffer. The input divider consists of R158, R159, R160 and R156, R157 is provided for calibration.

In the K Ohms function, the bottom of the input divider (R160) is removed from the common binding post and connected to the +7.0 volt reference supply. The divider now acts as the current supply for resistance measurements.

In the 10M Ohm function the bottom end of the range divider is connected to divider R152 and R154 which can be adjusted by R153 to provide 10M Ohm calibration.

When the AC Volts function is selected the input configuration is changed to an operational rectifier. A pair of rectifier diodes is placed inside a strong feedback loop. A negative feedback signal proportional to the input voltage is developed across R161, R162, R174 and calibration pot R34, which is fed to the A-D Amplifier.

INPUT FILTER

The output of the Range Divider is fed into a two pole, active filter consisting of R27, R28, C10, C11, C12 and C13. (Filter switch out.) The settling time is .25 sec and 60 Hz is attenuated about 20 db. With the Filter switch depressed, C10 and C13 are removed from the circuit and the settling time becomes 1 second and 60 Hz is now attenuated about 60 db. CR11 and CR12, together with R27 provide protection for both the filter and the Buffer amplifier from excessive voltage inputs. In the 10 volt range, R27 is switched out since the output impedance of the range divider is 1M Ohm and R27 is not needed.

BUFFER AMPLIFIER

Q77 is a low noise, low drive J-FET pair, operating in a common source configuration and serves as the input stage to the Buffer Amplifier configuration. R175 is the zero adjustment pot, which in conjunction with R176, R177 and R188 forms a network by which the initial offset of Q77 can be reduced to zero. The output of Q77 drives A1, a monolithic operational amplifier, which provides the bulk of the gain. C51 is placed around A1 to provide a smooth roll off through unity gain. Q79 is a common base output stage whose purpose is to raise the output impedance of the amplifier as high as possible. In order to avoid degrading the high output impedance, Q79 operates into a constant load current, Q80. The Buffer amplifier feedback loop is completed through diodes CR14 and CR15, which provide a voltage step around zero to drive the following polarity sensing circuit. R174 provides the load resistance for the amplifier.

When AC Volts function is selected, the buffer amplifier is connected as an operational rectifier with R24 as the input resistor, AC coupled through C9 and R29, R30, R31 and R32 as the negative feedback ranging resistors. Diodes CR14 and CR15 now act as an operational rectifier. The positive half cycles only flow through CR15 and R162 where they develop a half wave rectified DC voltage proportional to the average value of the AC input. The high output impedance of Q79 and Q80 aids appreciably in improving the linearity at low levels where the threshold voltages of CR14 and CR15 tend to lower the amplifier loop gain. The half wave rectifier output is smoothed by two stage RC filter R35, C19, R36 and C20 to provide a 1 volt full scale output for the A-D Converter. Because the input capacity of Q77, along with additional stray capacities, causes an additional pole in the loop response of the AC converter. Trimmer capacitors C14 and C15 are provided on the two lowest ranges to adjust the frequency response up through 20 kHz. The low resistances of R31 and R32 make this unnecessary on the two upper ranges.

8100A DIGITAL MULTIMETER OPERATIONAL THEORY

The 8100A consists of three main sections, referring to Figure 1 and the Schematic Drawings.

1. The Buffer section acts as a signal conditioner, capable of dividing voltage inputs, filtering and impedance conversion. The input divider also functions as a portion of the current source in the resistance ranges. (See Figure 2)
2. The Analog/Digital Conversion system, accepts the output from the Buffer and digitizes it using FLUKE'S Recirculating Remainder system of conversion. The unit samples three times a minute and recycles every 20 milliseconds.
3. The display section accepts the BCD output of the Analog to Digital Converter and puts it into ten line decimal output and displays the result on NIXIE tubes on a timed pulse basis.

In addition to the three main sections described above, the Power Supply serves dual functions. In addition to supplying the voltages required by the instrument it also contains an inverter that is used to both produce operating voltages for the instrument and supplies the clock or synchronization for timing the instrument.

Power for the 8100A is supplied by either the AC power line or via the internal battery pack, as furnished with the -01 option. When operated from line voltage transformer T101 provides two outputs. One output is rectified and filtered and used for the −18 volt supply in the instrument. The other winding provides a higher voltage which is rectified and used to charge the battery option, through DS11 which acts as a series limiting element.

The voltage supplied by the line voltage conversion is always greater than the voltage from the batteries, back biasing CR34 which prevents draining the batteries. The negative voltage, from either the batteries or the rectifiers CR1 and CR2, is regulated and filtered after passing through the protective fuse F2 and then on to supply the instrument all of it's negative voltage needs.

The −18 volts operates a 250 Hz inverter consisting of Q4, Q5 and a driver transformer T102. The output voltages from T102 are then conditioned to supply the remaining potential needs of the 8100A.

A high voltage winding (100v) operates a doubler rectifier circuit which provides 200v DC which is pulsed on every 4 milliseconds for 2 milliseconds. This provides a pulse for the last half of each time period of the instrument. This +200v DC is used to pulse the readout tubes.

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A-D CONVERTER (Figure 1)

The A-D Converter is synchronously operated. That is to say; it progresses through it's steps in time with an internal clock, which is the Power Supply Inverter (250 Hz). A Ring Counter fed by one of the outputs of T102, divides each cycle into five time periods of 4 milliseconds each. The first time period is the ZERO time, this is the time period when the offset is removed from the A-D Converter amplifier. During the remianing four time periods each of the four digits is digitized and then displayed. At the end of the last period, the Ring Counter supplies a synchronizing pulse through R68, C27, R69 and C28 to the Measure Store Multivibrator Q25 and Q26. It is the job of the Measure Store circuit to determine whether the A-D Converter will sample (Measurement Mode) the input voltage or continue to display the information held in storage (Storage Mode).

POLARITY SENSING

Q13 turns on only when a 1 period time pulse appears at its gate and in Measurement Mode. This activates the Polarity Sensing Circuit. If the voltage at R40 is positive (Negative instrument input) Q15 will conduct and the signal from the Measure Store Multivibrator (Q25) will cause FET switch Q16 to conduct placing input on the A-D Amplifier.

If the voltage sensed by R40 is negative (Positive input to the 8100) Q14 will conduct and the signal at the collector of Q14 and the pulse from the Measure Store Multivibrator Q25 will turn FET switches Q12 and Q17 on. The negative output of the Buffer will be applied through the scaling resistors R50 and R51 and switch Q12 to the negative input of the A-D Amplifier. The Polarity Detector operates only while the instrument is in the Measurement Mode of operation and serves no function in the Storage Mode.

During time period 1, the amplified remainder is applied to C35 Q35 is prevented from conducting during the first half of the time period by the clock signal which is coupled through CR36 to its gate During the second half of the period Q35 is on and the amplified remainder is applied to C34.

During the second time period, Q35 is off and Q36 is on which applies the remainder stored in C34 to be applied to the input of the Amplifier. Q39 is switched on and the remainder is now applied to C35, during the second half of the time period. Q39 is switched off during the third time period and Q37 and Q38 are switched on which applied the remainder stored in C35 to be applied to the amplifier input.

During the third time period, second half, the remainder is stored in C34.

During the fourth and last time period Q34 is switched on and the final remainder stored in C34 is applied to the input of the Amplifier.

ANALOG STORAGE

Clock pulses being applied through CR19 to Q28 allow conduction only during the second half of each time period. Q30 through Q33 are enabled only during the time period pulse corresponding to its gate connection.

During the last half of the 1 period the output of the Secondary Ladder is stored in capacitor C30. During the last half of the second period, the output of the Secondary Ladder is stored in C31. Etc.....

Q29 is enabled only when the instrument is in the Storage Mode and applied the output of each of the storage capacitors to appear at the input to the amplifier.

Analog storage is used only when the instrument is in the Storage Mode of operation as determined by the Measure Store Multivibrator.

MEASURE STORE MULTIVIBRATOR

The one shot multivibrator formed by Q25 and Q26 has dual synchronizing inputs. The Measurement Cycle (approx. 20 ms) is coincident with the conduction of Q25. The Storage Cycle (approx. 330 ms) is coincident with the conduction of Q26. The multivibrator is triggered at the end of each complete cycle by the negative edge of the 4th time period pulse. If C29 is sufficiently discharged, this negative pulse will cause the multivibrator to pulse, sending a 20 ms measure pulse to the Polarity Sensing circuit which starts a measurement cycle. If the multivibrator does not pulse the 8100 remains in Storage Mode.

DISPLAY

It should be noted that each readout tube is on only during the last half of its corresponding time period. (2 ms on and 18 ms off)

The BCD output of the A4 Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 3 the Decoder Driver will apply ground to the three line to all readout tubes. The 1 time period pulse will enable Q67 and Q71 which will allow the +200 volt pulse, which occurs only during the second half of each time period to light the three digit in V1.

EXAMPLE OPERATION (Figure 4) (Example voltage is .6532v)

Counter A4 is reset to zero as it is at the beginning of every time period by the pulse from A3A NAND gate.

The Ring Counter produces the ZERO pulse and Q18 and Q58 are turned on. Q58 connects C37, the zero holding capacitor, to the output of amplifier A2. Q18 connects the positive input of the amplifier to ground. This operation removes the offset for the remainder of the measurement cycle.

The Ring Counter produces the 1 time period pulse. It is necessary to assume that Q25 in the Measure Store Multivibrator is conducting. The 1 pulse will turn transistor Q13 on. Since the .6532 volts into the instrument is positive, the voltage across R40 will be negative. Q14 will conduct which will cause Q12 and Q17 to turn on. These transistors were enabled by the Measure pulse from the Measure Store Multivibrator. The negative voltage from the Buffer will be applied to the A-D Amplifier through scaling resistors R50 and R51. Q17 connects the positive input to the amplifier to ground via resistors R186 and R187 which provide offset correction voltage to the positive input.

With R98 200 kΩ in the feedback loop and R51 and R50 as the input resistance the gain of the amplifier is 70. Q52 is used as temperature compensation only.

With .6532 volts at the input terminal of the amplifier, the output will attempt to go to 40 volts to satisfy the loop gain, but will be prevented from going so high by the limiting action of Q76 and R110. The output will exceed 7.0 volts and cause Q61 to conduct, supplying current to the Voltage Controlled Oscillator.

The Voltage Controlled Oscillator, Q59 and Q60, will supply a series of pulses when supplied current. The repitition rate will be proportional to the current being supplied.

The pulses from the VCO are applied to the Counter A4, which is reset at the start of each time period. This counter translates the pulses into Binary Coded Decimal output. This BCD output is applied to the Ladder Switches and Drivers. As the BCD numerical value increases, the ladders produce 0.1 volt steps in their output. Thus in this case when the Primary Ladder output reaches .6 volts and is fed back to the input of the A-D Amplifier, the input difference to the amplifier becomes .0532 volts and the output of the amplifier will be less than 7 volts. When this occurs the Analog Comparitor Q61 does not furnish current to the VCO which causes it to stop pulsing.

The Decoder Driver translates this BCD output to decimal and produces a ground potential that is fed to all of the readout tubes 6 line. The +200 volts pulses only during the last half of the time period, so during the last half of the time period the readout tube is lighted. Only the 1 tube will light since it is the only one enabled by the 1 pulse via Q67 and Q71.

The Secondary Ladder feeds the Analog Storage circuit. Q28 is enabled only during the second half of each time period and Q30 is enabled by the 1 time period pulse. This causes C30 to be charged to .6 volts being furnished by the Secondary Ladder.

The remainder voltage during time period 1 was 0.532 volts at the input to the A-D Amplifier. This remainder is multiplied by the amplifier to 3.724 volts and appears across remainder resistors R99, R100 and R149. It is apparent that the total resistance is 14 kΩ and that 2 kΩ represents 1/7 of the total resistance. This means that one seventh of the voltage appearing across the total remainder resistance appears across R100. This means, in the example case, .532 volts. This voltage will be applied across C34 in the Sample and Hold Circuit by the 1 time period pulse enabling transistor Q35. CR36 allows Q35 to be enabled only during the second half of the time period.

SUMMARY:

The highlights of the action that has taken place during the first time period are as follows:

1. The .6 volts was digitized.
2. .6 volts was placed in Analog Storage.
3. The remainder voltage .532 was placed in storage.
4. The 6 was displayed during the last half of the time period by V1.

Time period 1 ends and transistor Q13 is no longer enabled as the 1 pulse is no longer furnished to it.

At the start of time period pulse 2 enables Q36 which applied the .532 volt remainder stored in C34 to appear at the input to the A-D Amplifier via Q18 which is enabled for the entire duration of The Measure Cycle. The .532 volts is amplified by 70 and once again the output of the amplifier exceeds the 7 volt reference causing Q61 to furnsih current to the Voltage Controlled Oscillator. The pulse train produced is translated to BCD output and the Ladders are switched up in 0.1 volt increments until .5 volts is fed from the Primary Ladder to the summing junction of the A-D Amplifier. The input to the amplifier at this time is 0.32 volts which results in an output from the amplifier that is less than 7 volts and Q61 cuts off. The BCD output from the A4 Counter is applied to the Decoder Driver and translated to decimal output, placing ground potential on all of the "5" lines to the readout tubes. The 2 pulses enables Q68 and Q72 during

the entire time period but the +200 volt pulse only occurs during the last half of the time period. Thus the readout tube V2 will display the "5" only during that last half of the time period.

The Secondary ladder will have an output of .5 volts at this time and it will be stored on capacitor C31 during the last half of the time period when Q28 conducts and Q31 is enabled by the 2 pulse.

The remainder, .032 volts will be amplified and divided by the remainder resistors and will be stored in the Sample and Hold circuit capacitor C35 via the enabled Q39 as .32 volts.

During period "3" Q38 will be enabled and apply the .32 volts stored there across the input to the A-D Amplifier through Q27.

The amplified voltage from the output of the amplifier will exceed the 7 volts of reference and Q61 will supply current to the Voltage Controlled Oscillator which will start a pulse chain. The pulses will be translated into BCD output. The BCD output will switch both Ladders and be decimalized by the Decoder Driver. When the output of the Primary Ladder reaches .3 volts the output of the amplifier will be less than 7 volts and Q61 will stop supplying current to the VCO. The decimalized "3" will appear as a ground potential on all of the 3 lines to the readout tubes. During the last half of the time period the +200 will pulse on and Q69 and Q73 being enabled by the 3 pulse will allow V3 to display the digit 3.

The .3 volts from the Secondary Ladder will be stored in Analog Storage capacitor C32 during the lasthhalf of the time period when Q28 is enabled and the 3 pulse has enabled Q32.

The remainder .02 at the input of the amplifier is amplified and appears across the remainder resistors and will be divided down to .2 volts and Q37 will be enabled causing this remainder to be stored in C34.

During time period 4 Q34 conducts applying the .2 volts stored in C34 to appear on the input to the A-D Amplifier. The output will exceed the reference voltage causing Q61 to supply current to the VCO which will start a pulse train. Counter A4 will count the pulses and translate them to BCD output. This BCD output causes the Ladder switches to operate and the output from the Primary Ladder is fed back to the summing point of the A-D Amplifier. When the output reaches .2 volts, the output of the amplifier is no longer higher than 7 volts and Q61 will stop conducting. The VCO stops pulsing and the Decoder Driver will translate the BCD output to decimal and apply ground potential to the 2 lines to all of the readout tubes. The 4 pulse will enable Q70 and Q74, which will allow the +200 volts to light the tube V4 when it pulses on during the second half of the time period. The Secondary Ladder will have an output of .2 volts which will be stored in Analog Storage capacitor C33, the 4 pulse having enabled Q33 and the second half time period pulse having enabled Q28.

This completes a Measurement Cycle. As the 4 time pulse goes negative returning to zero potential it will cause Q25 (Measure Pulse) to conduct, only if capacitor C29 is sufficiently discharged. In this case it would not be possible for the instrument to start another Measurement Cycle as C29 would be fully charged.

SUMMARY:

It will be noted that each increment of voltage has been stored in the Analog Storage capacitors as follows:

C30 .6 volts

C31 .5 volts
C32 .3 volts
C33 .2 volts

None of these stored voltages were used in the Measurement Cycle. C29 was fully charged and Q26 is conducting, which occurs during the Storage Cycles of the instrument. Q27 will be off and Q29 will be enabled until the Measure Store Multivibrator is operated again. Q26 will conduct for approximately 330 ms or about 16 cycles of the instrument. At that time C29 will be sufficiently discharged to allow Q25 to conduct when it receives a negative going pulse from the 4th time period pulse. Q25 will then conduct for approximately 20 ms or one Measurement cycle.

STORAGE CYCLE

The ZERO pulse will again cause the offset to be removed from the A-D Amplifier by placing C37 across the output of the amplifier and grounding the input, as the result of Q18 and Q58 conducting.

The 1 pulse will cause Q30 to enable and the voltage stored on C30 (0.6 volts) to be applied to the input of the A-D Amplifier through Q29, which has been enabled by the Measure Store Multivibrator.

The A-D Amplifier amplifies the .6 volts by 70 and the output of the A-D Amplifier exceeds the 7 volt reference causing C61 to conduct and supply current to the VCO. The VCO will start producing a pulse train. These pulses are counted and translated into BCD output by the action of Counter A4. The BCD output causes the Ladders to switch and increase their output by .1 volt per pulse. When the output of the Primary Ladder reaches .6 volts it will cause the A-D Amplifier to be satisfied and it will no longer have an output that is above the 7 volt reference of the instrument. The Secondary Ladder will have produced a .6 volt output which will be stored in C30 during the second half of the time period via Q28.

The Decoder Driver will have translated the BCD output to decimal and applied ground to all of the readout lamps on the 6 line. Q67 and Q71 are enabled by the 1 pulse and when the +200 volts pulses on, as it does during the second half of the time period V1 will display the 6.

During time period 2 Q31 and Q29 conducting will cause the .5 volts stored in C31 to appear across the input to the A-D Amplifier. The amplifier will have an output of more than 7 volts, which will cause Q61 to conduct and supply current to the VCO, which will produce a pulse train. The Counter A4 will count and translate the output to BCD. The Ladders will produce .1 volt of output for every pulse. The Primary Ladder being fed back to the input of the A-D Amplifier will cause the output of that amplifier to drop below 7 volts when .5 volts level is reached, which will cause Q61 to cut off and the VCO to stop producing pulses.

The Secondary Ladder will have produced .5 volts which will be stored on C31 during the second half of the time period by the conduction of Q28. The Decoder Driver will have placed ground potential on the 5 lines to the readout tubes. Q68 and Q72 will be enabled by the 1 pulse and during the second half of the time period the +200 volts will pulse on cuasing V2 to display the digit 5.

During the 3 time period, Q32 will be enabled placing the .3 volts stored in C32 to be applied to the A-D Amplifier. The output of the amplifier will exceed the 7 volt reference and Q61 will supply current to the VCO which produces a pulse train. The pulses will be counted and trans-

lated to BCD output. This BCD output will cause the ladder switches to operate and increase the output of both ladders to increase by .1 volt for every pulse of the VCO. When the output of the Primary Ladder reaches .3 volts the A-D Amplifier will be satisfied and its output will drop below 7 volts causing Q61 to stop conducting, and the VCO will stop pulsing. The output of the Secondary Ladder (.3 volts) will be stored on C32 during the second half of the time period through Q28 which conducts only during the second half of each time period.

The Decoder Driver will have translated the BCD output to decimal and placed ground potential on all of the 3 lines to the readout tubes. Q69 and Q73 will have been enabled by the 3 time pulse and the 3 will be displayed by V3 when the +200 volts pulses during the second half of the time period.

Time pulse 4 will cause the .2 volts on C33 to be placed on the input to the A-D Amplifier whose output will exceed the 7 volt reference. Q61 will conduct and the VCO will pulse causing the decoder outputs to step .1 volt for every pulse received. When the output of the Primary Ladder, which is fed back to the summing point, reaches .2 volts, the output of the amplifier will no longer be higher than the 7 volt reference and Q61 will stop supplying current to the VCO. The Secondary Ladder will charge C33 to .2 volts and the action of the Decoder Driver will cause ground potential to appear on all of the 2 lines to the readout tubes. Q70 and Q74 will be enabled and when the +200 volts pulses during the second half of the time period, V4 will display the 2.

SUMMARY:

The capacitors in the Analog Storage Circuit will contain all of the increments of the voltage that were digitized during the previous Measurement Cycle. The Sample and Hold Circuit is disabled during all Storage Cycles. Each digit is displayed only during the last half of each time period. During the Storage Cycle the Polarity Sensing Circuit is not enabled.

This completes the Storage Cycle and as previously explained, the instrument will enter another Storage Cycle unless the charge on capacitor C29 has decreased to a value low enough to cause the Measure Store Multivibrator to pulse. If the Multivibrator does pulse a new Measurement Cycle will start and the input will be sampled again.

TROUBLESHOOTING:

1. There are several ways of isolating the section of the 8100 that is malfunctioning. Observation of the readout and logical deduction baised upon the knowledge of the theory of operation may be adequate to sectionalize the trouble.

2. The Power Supplies are interrelated and to isolate troubles in this area it may be necessary to isolate the −18 volt supply. To do this, disconnect the +15 volt end of R5 and connect it to an external source, or disconnect R34 and place a 1330Ω ±1% resistor from the base of Q3 to ground.

3. The Input Buffer can be checked by measuring the voltage between TP9 and TP1 (ground), while measuring a voltage in the 1 volt DC range. The voltage measured should be the same as the input but in reverse polarity.

4. The Auto Zero circuit will mask many types of trouble, so to disable this circuit it will be necessary to jumper TP6 to TP7 and jumper −18 volts to TP8. The measurement will now have an offset but the Auto Zero will be disabled.

5. Storage Mode can be avoided and the instrument placed in continuous Measurement Mode by placing a jumper between TP4 and TP5.

6. Connect +15 volt supply to the junction of R60 and R61, the Ring Counter will stop and the instrument will no longer display anything in the readout tubes. All of the output lines should measure −18 volts at this time. Remove the jumper and measure the collector voltage with an oscilloscope, each collector should measure about .3 volts when the transistor conducts.

7. An excessive load on any Ring Counter output can cause it to oscillate. Spikes following the time pulse indicate that the Ring Counter is near oscillation.

8. Trailing edge droop on the time pulses is caused by low gain transistors Q20 through Q28.

9. The following procedure will check the operation of the A-D Amplifier;

   a. Disable the Ring Counter by placing a jumper from +15 volts to TP11.

   b. Disable the Measure Store Multivibrator by placing a jumper from TP4 to TP5.

   c. Enable the Polarity Sense by placing a jumper from Q31 source to Q31 drain.

   d. Remove Binary Counter A4.

   e. Measure the voltage between TP2 and TP1 (ground).

   f. Apply 100 mv increments of input to the 8100. The measured voltage should increase 350 mv for every 100 mv increment of input and will be of the same polarity.

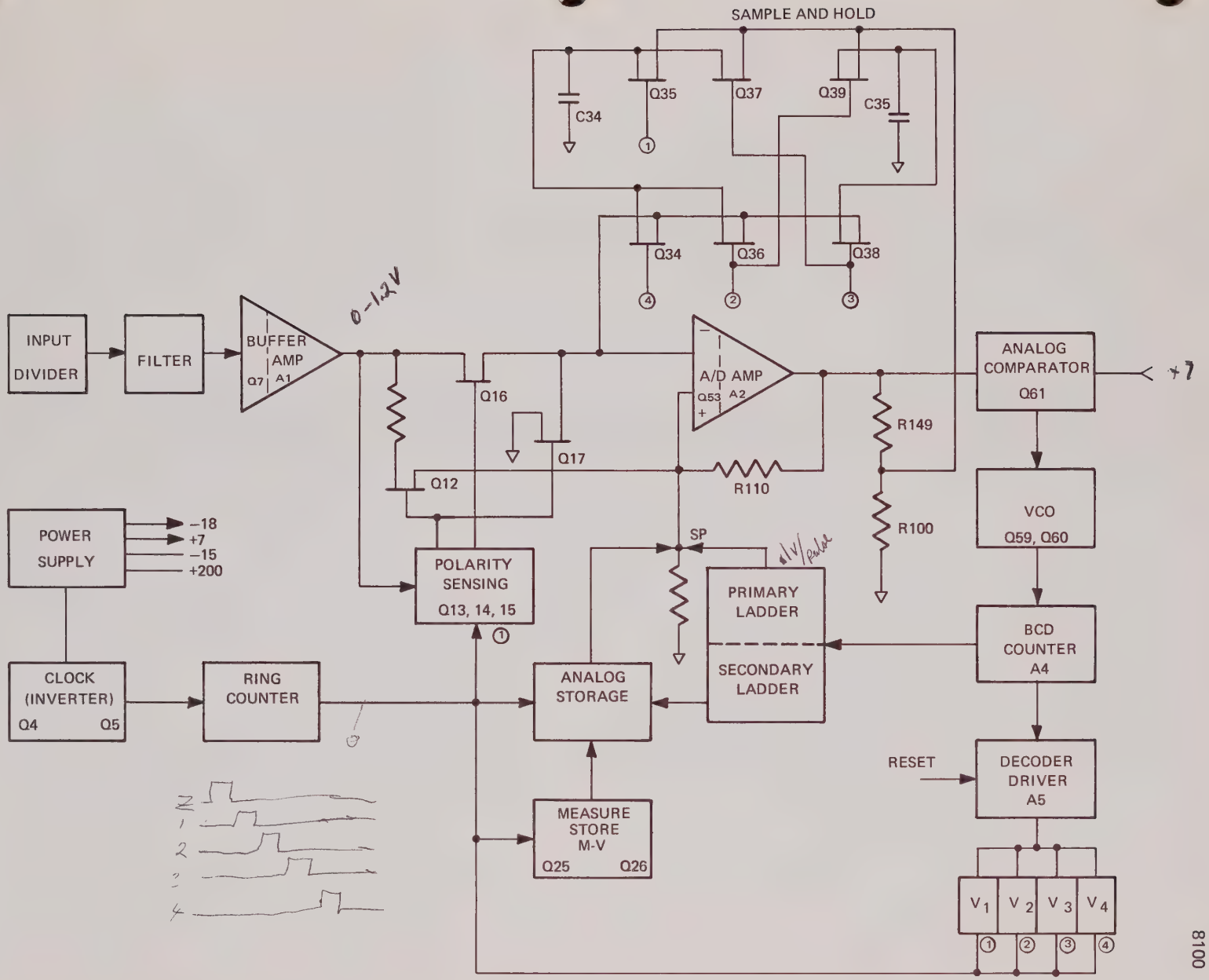


Figure 1. 8100 BLOCK DIAGRAM

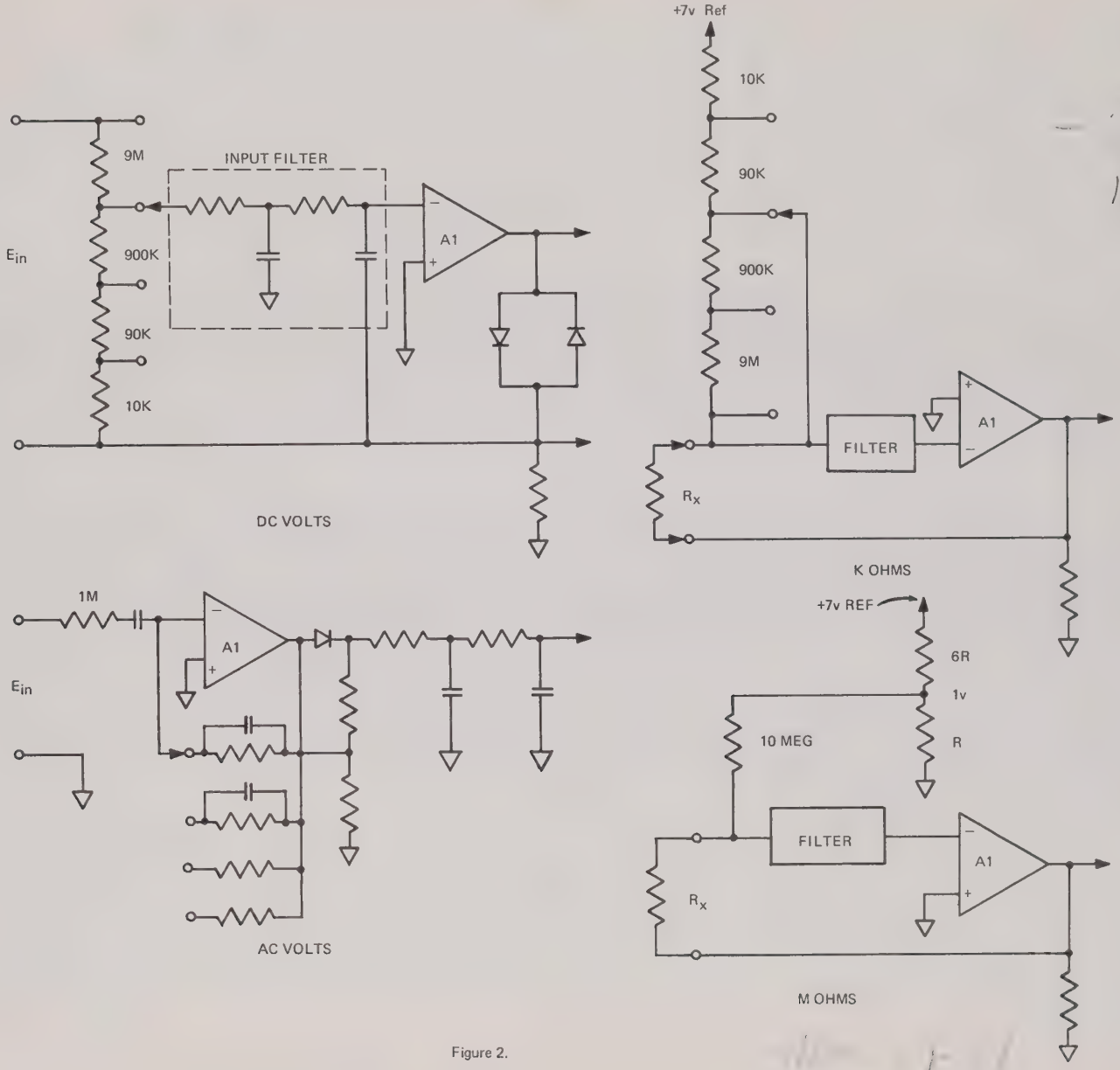

9M
INPUT FILTER
E_{in}
900K
90K
10K
A1
DC VOLTS
1M
E_{in}
A1
AC VOLTS
+7v Ref
10K
90K
900K
9M
FILTER
A1
R_x
K OHMS
+7v REF
6R
1v
10 MEG
R
FILTER
A1
R_x
M OHMS

Figure 2.

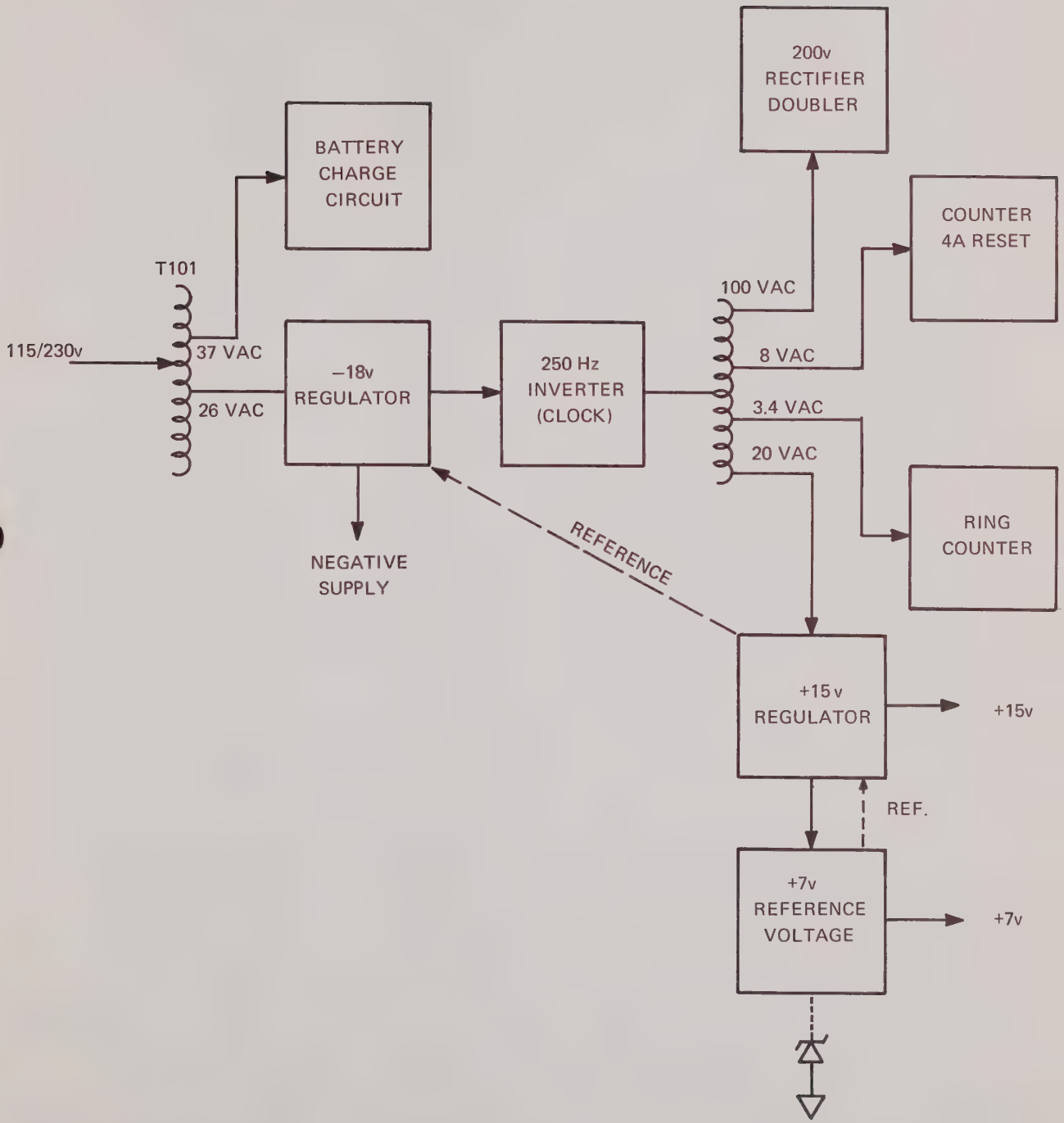


Figure 3. 8100 POWER SUPPLY

MEASURE MODE	ZERO	1	2	3	4
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
1 from Ring Counter enables Q13, polarity is determined and input FETs apply .6532 to A-D. 6 is digitized, remainder is stored in S & H C34. 6 is displayed and .6v stored in C30.		▬	▬		
Input is disconnected from A-D amplifier.					
.532v from C34 is applied to A-D input. 5 is digitized and remainder .32 is stored in S & H C35. 5 is displayed and .5v is stored in C31.			▬	▬	
.32 from C35 is applied to A-D amplifier. 3 is digitized and remainder .2 is stored in C34. 3 is displayed and .3v is stored in C32.				▬	▬
.2v from C34 is applied to A-D input and digitized. 2 is displayed and .2v is stored in C33.					▬

STORAGE MODE	ZERO	1	2	3	4
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
Q30 conducts and applies .6v from C30 to A-D amp. 6 is digitized 6 is displayed and .6v is restored to C30.		▬	▬		
Q31 conducts and applies .5v from C31 to A-D amp. 5 is digitized 5 is displayed and .5v is restored to C31.			▬	▬	
Q32 conducts and applies .3v from C32 to A-D amp. 3 is digitized. 3 is displayed and .3v is restored to C32.				▬	▬
Q33 conducts and applies .2v from C33 to A-D amp. 2 is digitized. 2 is displayed and .2v is restored to C33.					▬

NOTE: If C29 is sufficiently discharged, the negative going portion of the 4 pulse will trigger the Measure Store Multivibrator and a measure pulse will be generated and a measure cycle will be started. If not another storage cycle will start.

Figure 4.

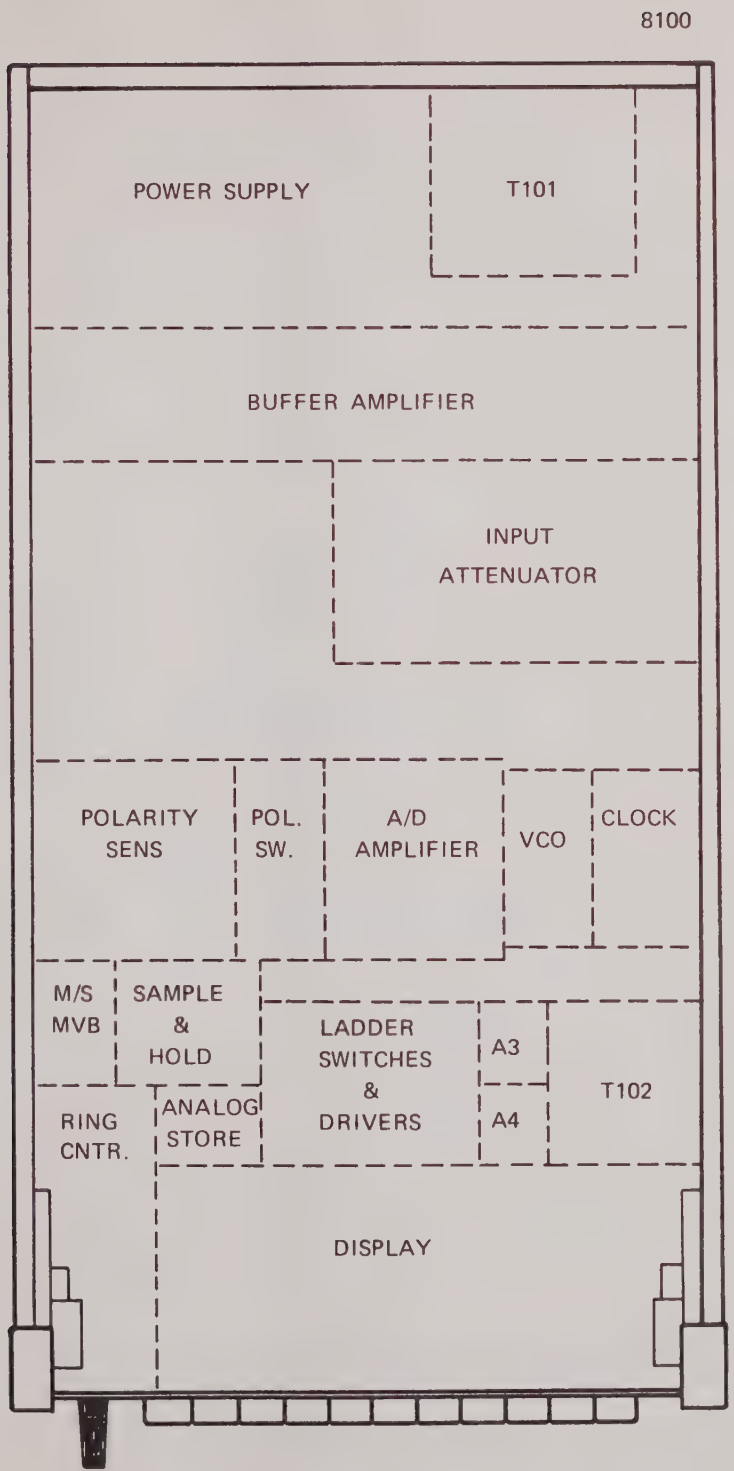
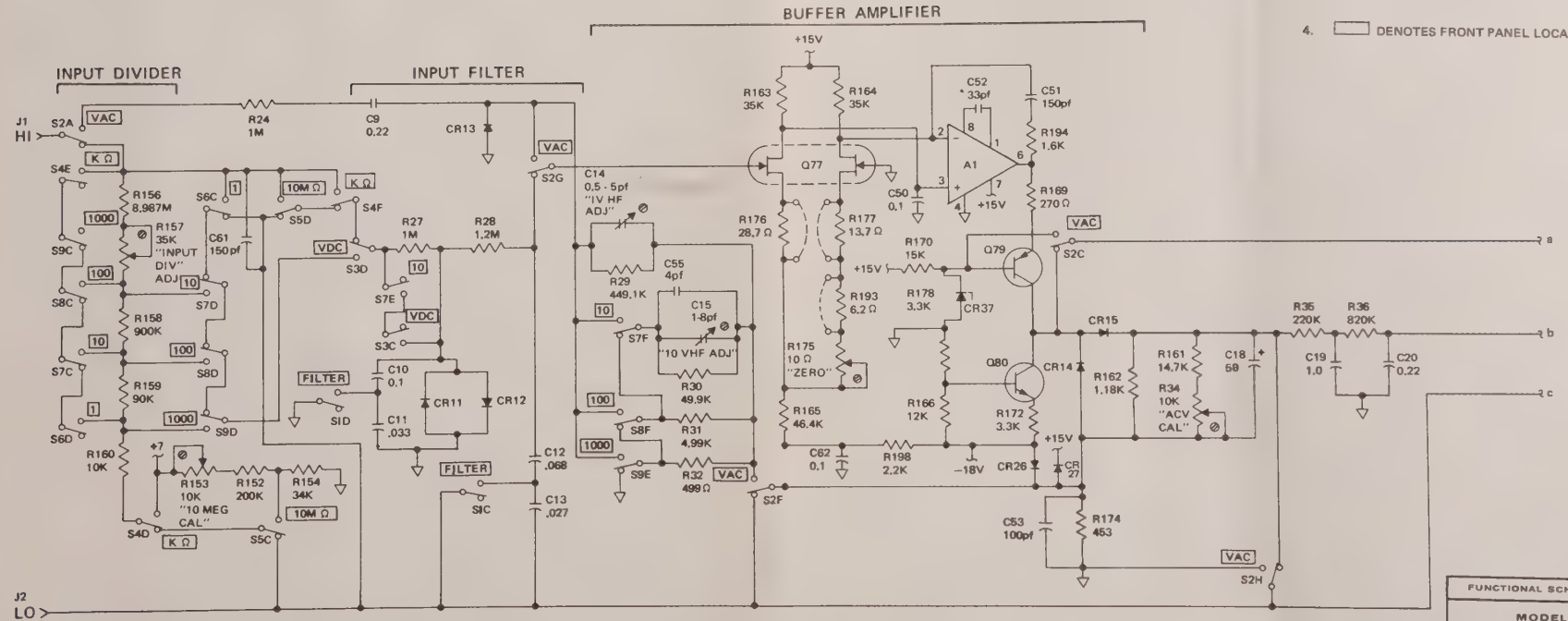


Figure 5. 8100 LAYOUT

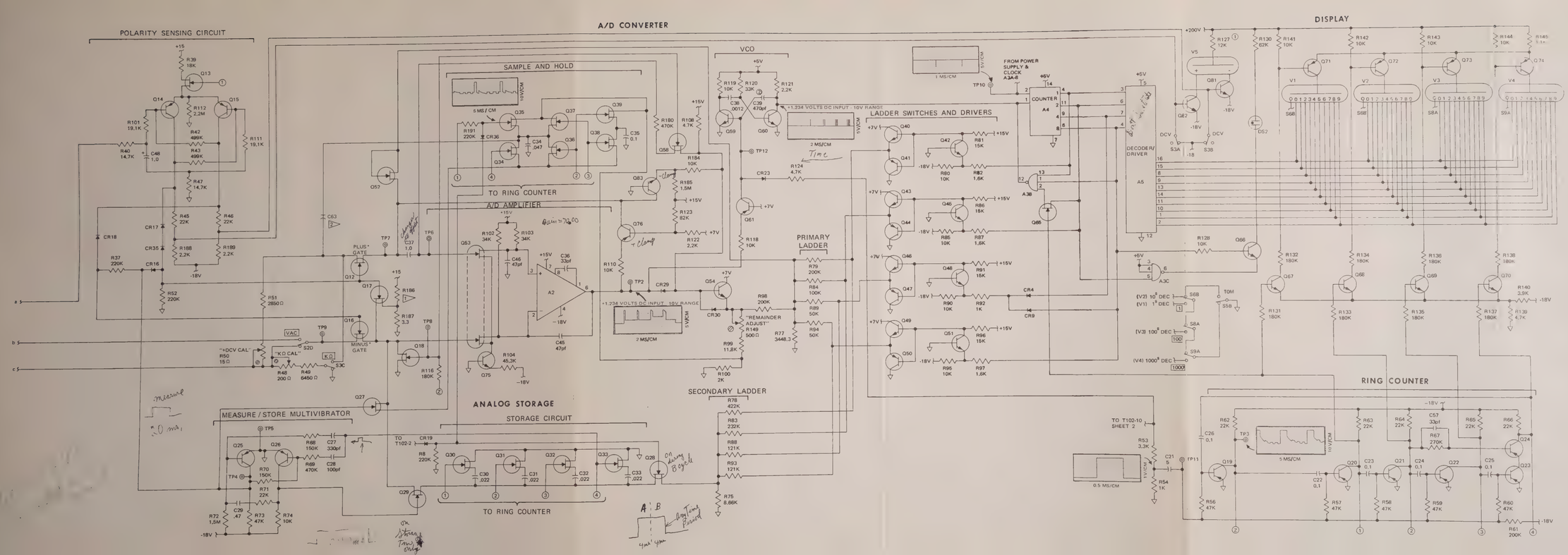
NOTES;

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.

BUFFER



FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER	
SCHEMATIC NO 1	
SER NO 123 & ON	REV 8
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



CHANGES:

1. R127 CHANGED FROM 22K TO 12K AT APPROXIMATELY S/N 400
2. C39 IS 220 pf IN SERIAL NUMBERS 124-131, 134, 135, 137, 139, 141, 142, 146, 147, 149-151, 157-159, 161-163, 165, 167-170.

NOTES:

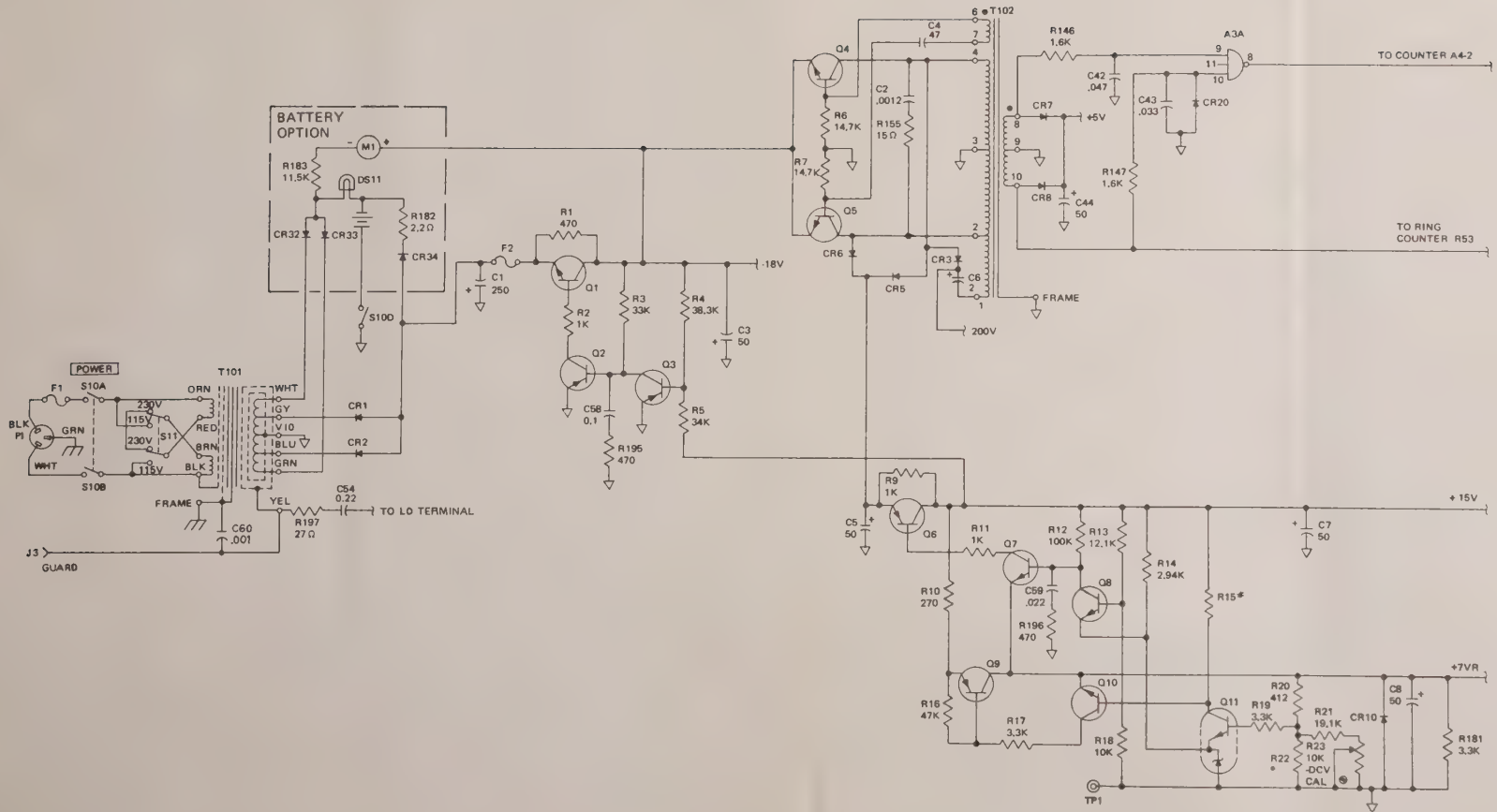
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⌀ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. ▷ R186 SELECTED IN FINAL CALIBRATION.
6. ▱ C63 SELECTED COMPONENT; NOT PRESENT ON SOME UNITS.
7. READOUT TUBE PIN LAYOUT:

	1 o	o 0
	2 o	o 9
	3 o	o A
RHD o	4 o	o 8 o LHD
	5 o	o 7
	6 o	o A

BOTTOM VIEW

8. * PLUS GATE ON WITH POSITIVE INPUT; MINUS GATE ON WITH NEGATIVE INPUT.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 810A	
DIGITAL MULTIMETER	
SCHEMATIC NO. 2	
SEE NO. 2A & 2B	REV. E
FLUKE	JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133



1. *RESISTOR VALUE SELECTED AT TEST OF Q11

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8100A
DIGITAL MULTIMETER

SCHEMATIC NO 3

SER NO 123 & ON

REV B

FLUKE JOHN FLUKE MFG CO., INC.
P O Box 7428 Seattle Washington 98133

JOHN FLUKE MFG. CO., INC. ■ MODEL **8300A**

FLUKE

DIGITAL VOLTMETER

FEATURES

BASIC:

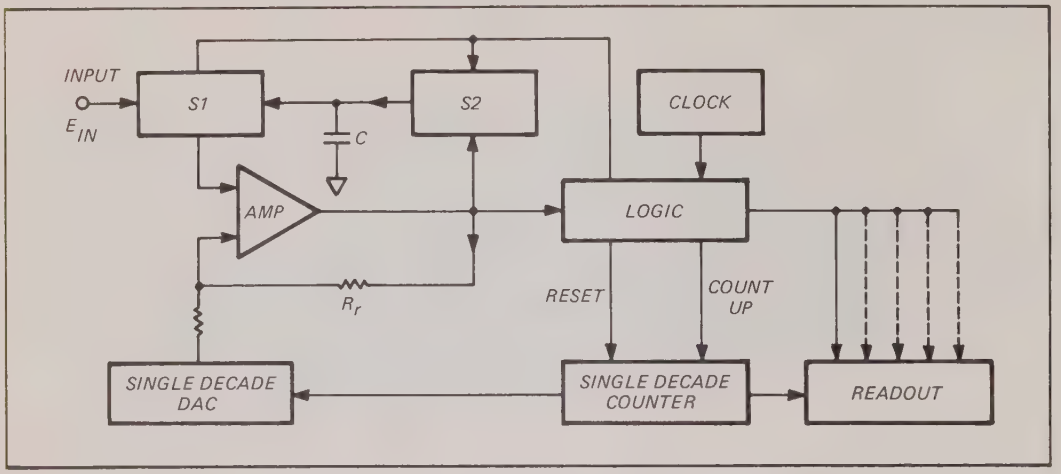
- *3 RANGES DC TO ±1100V — AUTO RANGE AND AUTO POLARITY*
- *"RECIRCULATING REMAINDER" * A/D CONVERSION FOR HIGH RELIABILITY*
- *FULL 5 DIGITS + "1" FOR 20% OVERRANGING*
- *ACTIVE 3-POLE SWITCHABLE FILTER WITH 60 Hz NOTCH*
- *40 READINGS PER SECOND FOR SYSTEMS APPLICATIONS*

OPTIONS:

- *AC VOLTAGE MEASUREMENTS IN 4 RANGES FROM 0 TO 1100 VOLTS*
- *MILLIVOLT/FOUR TERMINAL OHMS IN ONE OPTION*
- *ISOLATED EXTERNAL REFERENCE ALLOWING 4-WIRE BIPOLAR RATIO MEASUREMENT*
- *ISOLATED DIGITAL DATA OUTPUT IN SERIAL OR PARALLEL FORMAT*
- *ISOLATED REMOTE CONTROL*

* Patent Pending

The 8300A is a versatile digital voltmeter with five full decades of digits plus a 6th digit for 20% overrange. Its mainframe will accept all options at any time, in any sequence for expansion from a bench DVM into a bench or systems multimeter.



Fluke's new and unique "Recirculating Remainder" A/D conversion technique is used in the 8300A. Its conversion circuitry periodically samples the input and serially digitizes the sample.

At the beginning of a conversion cycle, switch S1 connects E_{in} to the AMPlifiers input. The amplifier acts first as a comparator with its output stimulating the LOGIC to instruct the SINGLE DECADE COUNTER to count up the SINGLE DECADE DAC until its output equals the most significant digit (MSD) of the input. The remainder (difference) voltage of E_{in} – MSD is multiplied by 10 because remainder resistor R_r provides feedback for precise control of amplifier gain following determination of the MSD. The amplified remainder, 10 (E_{in} – MSD), is stored on capacitor C via switch S2 and the registered count is transferred to the READOUTs first digit.

Following display, the counter is reset to zero and S2 opened. S1 disconnects from E_{in} and connects the voltage on C to the amplifier. Second digit conversion is accomplished with the same circuits and procedures used to determine the first digit. The registered count is transferred to the readouts second digit and a new remainder stored on C.

Conversion is repeated three more times in the FLUKE 8300A using remainder voltages stored from the immediately preceeding conversion.

"Recirculating Remainder" conversion circuitry is characterized by a low total parts count and extremely low power consumption.

Autoranging is a standard feature of the 8300A although preselected ranges may be programmed manually via front panel pushbutton switches or with the remote control option. Functions are also manually programmed at the front panel or remotely by option. The pushbutton switches are interlocked to prevent simultaneous operation of incompatible functions or ranges. All switches are installed in the basic 8300A whether the function is or not.

The left side of the readout illuminates to display the function called, polarity for DCV and MV, presence of filter and an overload warning. The readout does not illuminate for optional functions that are not installed. The readouts neon tubes are non-blinking and decimal point positioning is automatic.

Measurement of noisy inputs is enhanced by manual or remote (optional) programming of the 8300A's active 3-pole filter. The filter has a notch at 60 Hz and is buffered to eliminate "kick-back" and input impedance changes.

The 8300A's sample rate can be manually varied from the front panel or it can be remotely controlled (optional).

Full guarding is accomplished by box-in-a-box construction and use of a FLUKE custom-designed isolating power transformer. Guarding is not compromised when the isolated Data Output and Remote Control units are added.

Calibration is accomplished through the guard via labelled ports.

ANALOG OPTIONS

All options may be installed in the field or factory for the same price. The analog options are fully within the guard, their installation automatically enables the appropriate function light of the display. Options are calibrated and ready for immediate use when field installed.

AC volts features a 50 Hz to 20 KHz midband with good accuracy to 30 Hz and 100 KHz. The AC converters output is the average rectified value of the AC input scaled to digitize as the RMS value of a sine wave.

Mv/Ohms extends the DC capability of the 8300A to 100 mv at full range with 1 uv of resolution. It includes 5 resistance ranges, using a modified four-terminal configuration on the two lowest.

External Reference can be used for true four-terminal ratio or for systems measurements related to a master reference.

DIGITAL OPTIONS

Data Output is completely isolated from the analog input and is available in a 8–4–2–1 BCD logic level format. Data is transferred serially via guarded toroids from the 8300A to the Data Output unit. Single decade code conversion and serial-character, parallel-bit acquisitions are unique capabilities in addition to standard full parallel output.

Remote Control is fully isolated from analog input and may be fully isolated from the Data Output unit but is normally used in conjunction with it. Control is exerted by logic levels or contact closures. Isolation from analog circuitry is accomplished through the use of light-emitting diodes and photo-transistors.

SPECIFICATIONS

DC VOLTS

RANGES . . . . . ±10V, ±100V and ±1000V. 20% overrange capability (1100V maximum)

POLARITY: . . . . . Automatic, instantaneous selection and display.

RANGE SELECTION: . . . . . Manual and autorange standard (Remote optional)

RESOLUTION: . . . . . 0.001% of range (100 uv on 10V range)

ACCURACY:

24 hours, 23°C ±1°C . . . . . ±(0.005% of input + 0.001% of range)
30 days, 20°C to 30°C . . . . . ±(0.01% of input + 0.002% of range)
90 days, 20°C to 30°C . . . . . ±(0.01% of input + 0.003% of range)

TEMPERATURE COEFFICIENT

0°C to 20°C, 30°C to 50°C . . . . . ±(0.0007% of input + 0.0003% of range)/° C

INPUT RESISTANCE:

10V RANGE . . . . . 10,000 megohms minimum.
100V & 1000V RANGES . . . . . 10 Megohms.

FILTER . . . . . Switch selected 3 pole active filter standard (remote control optional)

RESPONSE TIME:

INCLUDING POLARITY CHANGE . . . . . To within 0.01% of step function change.
25 ms maximum unfiltered. (No settling time required for input applied coincident with read command. Time given is digitizing time only.)
500 ms maximum filtered.
NOTE: Filter settling time unaffected by source impedance.

REJECTION:

	DC	AC
Normal Mode (Filtered)	–	>60 db, above 50 Hz
Common Mode (Unfiltered)		
1 KΩ unbalance in either lead	>140 db	>100 db, 60 Hz and above.
100Ω unbalance in either lead	>160 db	>120 db, 60 Hz and above.
Common Mode (Filtered)		
1 KΩ unbalance in either lead	>140 db	>140 db, 60 Hz and above.

MAXIMUM NORMAL MODE VOLTAGE . . . . . 50% of range, peak AC.

MAXIMUM COMMON MODE VOLTAGE . . . . . 1000V DC or peak AC.

ADDITIONAL SPECIFICATIONS BASIC DC UNIT 1100V DC or RMS (1500V peak AC) overload with no damage (any range).
Input capacitance < 100 pf.
Input offset current less than 50 pa on any range.

DC MILLIVOLTS (USING MV/OHMS OPTION 8300A-02)

RANGES . . . . . ±100 mv and ±1000 mv. 20% overrange capability
(Up to 1100V overload with no damage)

POLARITY . . . . . Automatic, instantaneous selection and display.

RANGE SELECTION . . . . . Manual and autorange standard (Remote optional)

RESOLUTION . . . . . 0.001% of range
(1 uv on 100 mv range)

ACCURACY

90 days, 20°C to 30°C . . . . . 1000 mv range ±(0.01% of input + 0.003% of range)*

100 mv range ±(0.01% of input + 0.01% of range)*

*ZERO STABILITY (after 30 minute warmup) Better than 8 uv for 90 days. (Front panel millivolt zero control provided to compensate for external thermal EMFs, etc.)

TEMPERATURE COEFFICIENT:

0°C to 20°C, 30°C to 50°C . . . . . 1000 mv range ±(0.0007% of input + 0.0003% of range)/°C

100 mv range ±(0.0007% of input + 0.0005% of range)/°C

INPUT RESISTANCE:

1000 mv Range . . . . . 1000 megohms minimum.
100 mv Range . . . . . 100 megohms minimum.

RESPONSE TIME: (Including polarity change, to within 0.01% of step function change)

1000 mv Range . . . . . 1 second maximum.

100 mv Range . . . . . 3 seconds maximum.

NOTE: Response time figures applicable for source resistance up to 50 KΩ

REJECTION:

	DC	INTERFERENCE FREQUENCY	
		50 Hz	60 Hz
Normal Mode	–	> 55 db	> 60 db, 60 Hz and above
Common Mode 1 KΩ unbalance in either lead	> 140 db, DC to 60 Hz		

MAXIMUM INPUT VOLTAGE . . . . . 1100 VDC or RMS (1500V peak AC) overload with no damage (any range)

AC VOLTS (USING AC OPTION 8300A-01)

RANGES . . . . . 1V, 10V, 100V and 1000V
20% overrange capability (1100V RMS maximum)

RANGE SELECTION . . . . . Manual and autorange standard (Remote Optional)

RESOLUTION . . . . . 0.001% of range (10 uv on 1V range)

ACCURACY:
20°C to 30°C

	INPUT VOLTAGE	
FREQUENCY RANGE	.001V – 500V	500 – 1000V
50 Hz – 20 KHz	±(0.1% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	±0.15% of input
20 KHz – 50 KHz	±(0.2% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	±0.2% of input **
30 – 50 Hz and 50 KHz – 100 KHz	±(0.5% of input +0.005% of range)* +0.02% of range) 30 days +0.03% of range) 90 days	**

* Using front panel AC zero control periodically (typically 8 to 24 hours after 30 minute warmup) 30 and 90 day specifications apply if front panel zero is not used.

** Input Volt–Hertz product should not exceed 2×10^7.

TEMPERATURE COEFFICIENT

0°C to 20°C, 30°C to 50°C . . . . . ±(0.002% of input + 0.001% of range)/°C.

INPUT IMPEDANCE

(All Ranges) . . . . . 1 megohm shunted by < 100 pf

RESPONSE TIME:

(To within 0.1% of step function change) . . . . 500 ms maximum.

MAXIMUM INPUT VOLTAGE . . . . . 1100V RMS
(Up to ±1100V superimposed DC is allowed if the peak voltage does not exceed 1500V).

REJECTION:

Common Mode (DC to 60 Hz) . . . . . 100Ω unbalance in either lead. > 120 db

Maximum Common Mode Voltage . . . . . 1000V DC or peak AC.

OHMS (USING MV/OHMS OPTION 8300A-01)

RANGES . . . . . 1KΩ, 10KΩ, 100KΩ, 1000KΩ, 10MΩ. 20% overrange capability all ranges.

RANGE SELECTION . . . . . Manual and autorange 1 KΩ through 1000KΩ ranges.
10 MΩ range selected manually.
(Remote selection optional all ranges).

RESOLUTION . . . . . 0.001% of range
(10 milliohms on 1K range)

ACCURACY:

90 days, 20°C to 30°C . . . . . 1 KΩ, 10 KΩ, 100 KΩ Ranges
±(0.01% of input + 0.003% of range)

1000 KΩ Range
±(0.02% of input + 0.003% of range)

10 MΩ Range
±(0.05% of input + 0.003% of range)

TEMPERATURE COEFFICIENT:

0°C to 20°C, 30°C to 50°C . . . . . KΩ Ranges
±(0.0007% of input + 0.0003% of range)/°C

10 MΩ Range
±(0.003% of input + 0.003% of range)/°C

MEASUREMENT CURRENT:
(And Mode)

Range (KΩ)	1	10	100	1000	10 MΩ
Current (ua)	1.1 ma	110	100	10	1
Mode	4 terminal		2 terminal		

NOTE: Power dissipated in unknown resistor is only 1.2 milliwatts at 1 KΩ

RESPONSE TIME:
(To within 0.01% of step function change)

RANGE	UNFILTERED	FILTERED
1 KΩ 10 KΩ	1 sec	1.5 sec
100 KΩ, 1000 KΩ	25 ms *	
10 MΩ,	50 ms *	

* Includes 25 ms digitizing time-- No settling time required on 100 K & 1000K ranges for input applied coincident with read command.

MAXIMUM INPUT VOLTAGE . . . . . 30V RMS opens protective fuse.

4-WIRE RATIO (USING ISOLATED EXTERNAL REFERENCE OPTION 8300A-05)

RANGES:

MODE	RATIO RANGE ($\frac{A}{B}$)	READING	V INPUT (A)	V REF. (B)
DC/DC	0 ± 1.0	0 ±10.0000	0 ±10V	+2V to +10.5V Standard
	0 ± 10	0 ±100.000	0 ±100V	
	0 ± 100	0 ±1000.00	0 ±1000V	
MV/DC	0 ±0.01	0 ±100.000	0 ±100 mv	
	0 ±0.1	0 ±1000.00	0 ±1000 mv	

NOTE: DC External Reference may also be used for AC measurements.

20% overranging, autorange and autopolarity operation apply to V input for all modes above as applicable.

ACCURACY:

90 days, 20°C to 30°C . . . . . Same as basic DC except "% of range" must be modified to "% $\left(\frac{10V}{V\ REF}\right)$ of range".

Example: DC/DC ±(0.01% of reading + 0.003% $\left(\frac{10V}{V\ REF}\right)$ of range)

EXTERNAL REFERENCE INPUT SPECIFICATIONS:

Input Impedance . . . . . 1 megohm.

Response Time . . . . . To within 0.01% of step function change (2 seconds).

NORMAL MODE REJECTION: . . . . . > 30 db at 60 Hz.

ISOLATION: . . . . . Algebraic sum of V input + common difference voltage not to exceed 13V on 10V range and MV ranges.
(input & reference commons)

GENERAL:

DISPLAY	Function/polarity display block plus six digit in-line neon readout.
DIGITIZING TIME	25 ms maximum.
SAMPLE RATE	Front panel variable from 10 readings/sec to 1 reading/3 sec + "EXT" (External Control) position. 40 reading/sec under external control through the Data Output Unit.
MAXIMUM INPUTS:	
"HI" to "LO"	See individual function specifications.
"LO" to "GUARD"	100V
"GUARD" to "GROUND"	1000V DC or peak AC.
TEMPERATURE RANGE	Operating 0°C to 50°C Storage −40°C to +75°C
HUMIDITY RANGE	Operating < 70% relative humidity; 25°C to 50°C < 80% relative humidity; 0°C to 25°C
ALTITUDE	Operating 10,000 Feet. Non Operating 50,000 Feet.
SHOCK & VIBRATION	Meets requirements of MIL-T-21200G and MIL-E-16400F.
POWER	115/230V, ±10%, 50-440 Hz line, 20 watts with all options.
WARMUP TIME	30 minutes to meet all specifications.
WEIGHT	15 lbs basic. 19 lbs with all options.
SIZE	3.5" high by 17.5" wide by 15" deep (see outline drawing)

PRICE:

8300A	$1295
8300A-01 AC	$450
8300A-02 MV/Ohms	$350
8300A-03 Data Output Unit	$500
8300A-04 Remote Control Unit*	$200
8300A-05 External Reference (Ratio) (requires -07)	$200
8300A-06 Rear Input (requires -07)	$15
8300A-07 Rear Terminal Accessory**	$25

*Remote control unit requires Data Output Unit, 8300A-03. If Remote Control Unit only is needed, consult factory.

**-07 required with -05 or -06.

NOTE: When ordering an option for field installation, prefix the option number with "8300A" and suffix it with "K". e.g. 8300A-01K.

REMOTE CONTROL (Using REMOTE CONTROL option 8300A-04)

INPUTS		LINES	LOGIC LEVELS	
Function:	DCV, MV, ACV, KΩ, MΩ Filtered, External Reference	7	0 to +0.5V (or contact closure)	+5V (or open)
			Function Called	Function inactive
Range:	1, 10, 100, 1000 uncoded	4	Range Called	All lines open Autorange

Input is series 930 DTL

INTERLOCKS	Interlocks are provided to disallow multiple function or range calls for incompatible combinations.
POWER	+5V power available from Data Output Unit (May be externally powered -- 5V DC at 150 ma required).
ISOLATION	All CMRR specifications apply with RCU installed. 1000 VDC or peak AC may be applied between RCU common and input "LO".

8300A SPECIFICATIONS

DATA OUTPUT UNIT: (USING DATA OUTPUT OPTION 8300A-03)

OUTPUTS	LINES	LOGIC LEVELS	
		0 to +0.5V	+5V
FUNCTION: DCV, MV, ACV, KΩ, MΩ Filter, External Reference	7	Function inactive.	Function called.
RANGE (Coded): 1 = 00, 10 = 01, 100 = 10, 1000 = 11 [1]	2	Logic 0	Logic 1
POLARITY:	1	Negative	Positive
6 DIGITS (Including "Overrange "1") Binary-Coded Decimal 8-4-2-1	21	Logic 0	Logic 1
DATA READY (Print) COMMAND	1	Data Ready	Data Blanked
OVERLOAD FLAG	1	No Overload	Overload
+5V REF & RETURN (TO POWER RCU)	2	----	----
INPUTS		0 to +0.5V	+5V (or open)
EXT. TRIGGER (Read Command)	1	+5V pulse > 1 usec	
SAMPLE TIME (Programmed Timeout)	1	Fast	Normal
INHIBITS (Address Lines For) (Serial Acquisition)	10	Inhibit	Normal

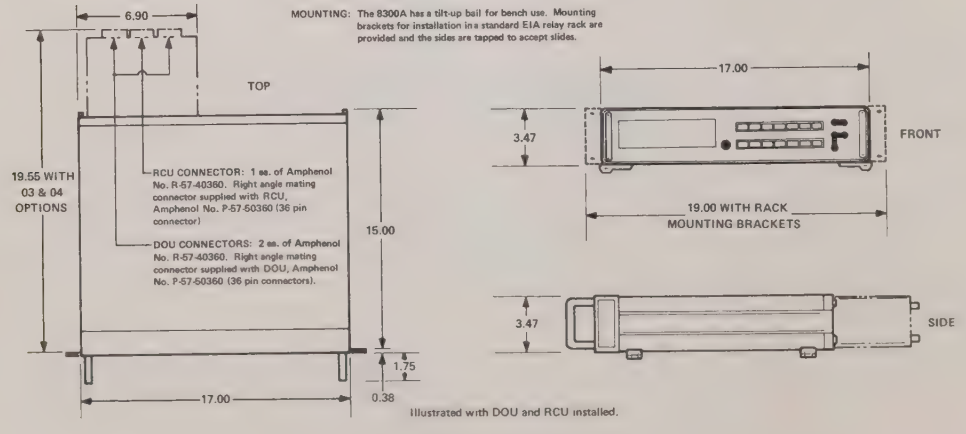
NOTE: 8 additional output lines and 4 input lines provided for code conversion of output data – contact factory. Output is series 930 DTL with 6K collector resistors.

OUTPUT FORMAT . . . . . Complete parallel and addressable for parallel bit-serial character in multiples of 4 bits.

BLANKING . . . . . All outputs are high during conversion and programmed time outs – outputs enabled at time "Data Ready" flag appears.

POWER . . . . . +5V DC available as output to power remote control unit if desired.

ISOLATION . . . . . All CMRR specifications apply with DOU installed. 1000 VDC or peak AC may be applied between DOU common and input "LO".


6.90
TOP
19.55 WITH 03 & 04 OPTIONS
RCU CONNECTOR: 1 ea. of Amphenol No. R-57-40360. Right angle mating connector supplied with RCU, Amphenol No. P-57-60360 (36 pin connector)
DOU CONNECTORS: 2 ea. of Amphenol No. R-57-40360. Right angle mating connector supplied with DOU, Amphenol No. P-57-60360 (36 pin connectors).
15.00
1.75
0.38
17.00
MOUNTING: The 8300A has a tilt-up bail for bench use. Mounting brackets for installation in a standard EIA relay rack are provided and the sides are tapped to accept slides.
17.00
3.47
FRONT
19.00 WITH RACK MOUNTING BRACKETS
3.47
SIDE

Illustrated with DOU and RCU installed.

Litho in U.S.A.

FLUKE

JOHN FLUKE MFG. CO., INC.
P. O. BOX 7428 - SEATTLE, WASHINGTON 98133 ■

TEL. (206) 774-2211
TWX 910-449-2850
Cable: FLUKE

II. BLOCK FUNCTIONS: (Figure 1)

A. Power Supply

The Power supply furnishes five voltages used in the insturment. +18, −18 operating supplies, +190 volt readout tube supply, +5 volt logic supply and +7 volt reference supply. Provisions are made for auxilary supply of 5 volts required in the Data Output Unit option.

B. Buffer

The Buffer board assembly includes Function switching components. It has an input impedance that is greater than 10^{12} with an insertion current less than 50 pa. The Input Attenuator offers three ratios of voltage division 1/1, 1/10 and 1/100. Input limiting is provided to prevent damage to the instrument in any range with up to 1100 volts applied.

The total gain of the Buffer is 1 inverted with a low impedance output. Input filtering is included in this assembly which consists of a 60 Hz notch filter and a 3 pole low pass (30 Hz) filter. All frequencies above 50 Hz are attenuated by more than 60 db.

C. Logic Section

A clock which operates at a frequency of 333 Hz produces a pulse train of 1.5 ms pulses, provides the timing for the entire instrument.

A 6 State Register divides the Clock pulses into six discrete time periods, which correspond to the ZERO time and the five digit times used in the instrument.

Current Controlled Oscillator provides a series of pulses that correspond to the digitalized value of the digit being converted from analog to digital value.

16 State Binary Counter receives the pulses from the Current Controlled Oscillator and converts them to Binary Coded Decimal (BCD) output in the standard 1-2-4-4 output.

Manual Range Controls are interlocked mechanically and electrically so as to provide priority to manual selections of function and range, preventing erronious dial function or range commands.

Auto Range Controls are provided to accomplish automatic selection of the proper range via reed relays and functional logic packs.

Sample Oscillator provides a variable sample rate from once every 3 seconds to once every 100 milliseconds. Provisions for external sample rates up to 25 milliseconds are included.

Anode Strobing circuit pulses each readout tube on for 1.5 ms during the appropriate time period of each complete cycle of the instrument. This means that during every 18 millisecond recycle period of the instrument each readout tube is only on for 1.5 milliseconds.

Sample and Hold circuitry is used during the Measurement cycle of the instrument when the input is sampled and is first digitized.

Logic Section provides the solid state switching commands for both range and function controls.

D. A-D Converter

Inverting Amplifier is used only when the input voltage being measured is negative. When the input to the instrument is positive, FET switches cause the output of the Buffer to bypass the Inverting Amplifier.

Polarity Detector circuitry automatically detects the polarity of the input signal and provides outputs for the logic switching of the Inverting Amplifier.

A-D Amplifier has two fixed gains, and is one of the key elements in the Recirculating Remainder system of analog digital conversion system.

Ladders and Switches provide a voltage back to the summing junction of the A-D Amplifier and also a discrete voltage that is stored in the Analog Storage for use when the instrument is in the Storage Mode of operation.

Sample and Hold circuitry provides storage for the remainder voltages while the instrument is in the Measurement Mode of operation.

Analog Comparitor provides current to the Current Controlled Oscillator whenever the output of the A-D Amplifier exceeds the reference voltage of 7 volts.

Current Controlled Oscillator provides a pulse train whose output pulses are proportional in repitition rate to the current being supplied it. The pulses supplied by this oscillator are fed to the 16 State Binary Counter for decoding.

E. **AC Converter**

The input impedance is 1 megohm into the inverting amplifier. The gain is controlled by feedback switching. Rectification is accomplished by dual section half wave diodes.

Filtering is accomplished by a 3 section RC filter combined with large feedback loop capacitors. The output of the filter is fed to a times 10 Inverting Amplifier which feeds the A-D Converter of the instrument.

F. **Millivolt/Ohms Converter**

In millivolt operation a chopper stabelizer operational amplifier is used which feeds an intergrated circuit operational amplifier with a gain of 10 on the 1000 millivolt scale and a gain of 100 on the 100 millivolt scale. The output of the millivolt section of the converter is 0 to 12 volts DC.

In Ohms operation the converter uses the +7 volt reference to supply current to the unknown resistance and the voltage drop across that resistor is translated by the instrument into ohms values. The instrument input is so configured as to provide modified four terminal resistance measurements for additional accuracy.

G. **External Reference**

This option provides a means of referencing the instrument to external sources from 2 to 10.5 volts via a chopper stabelized operational amplifier to increase the isolation between the system under measurement and the 8300.

H. **Remote Control Unit**

The Remote Control Unit can be operated from either 5 volt logic or from relay closures and will give full control of function and Range of the instrument. Four lines provide control of the range functions and 7 lines provide function control. Light operated diodes give this option the very high degree of isolation required.

I. **Data Output Unit**
Will provide parallel, serial or parallel bit format output. Transformer coupling provides the isolation required. This unit has a high degree of flexibility for properly mating with the broadest variety of configurations.

III. SUB-SECTION FUNCTIONS

A. Power Supplies (Figure 2)

The primary windings are so configured as to provide either 115 VAC or 230 VAC input power which is selected by a switch on the rear panel.

The +18 volt supply is zener regulated and provides the initial reference for the other supplies, so if trouble exists in the +18 supply it is reasonable to expect that all of the other supplies will also show a problem.

The −18 volt supply is referenced to the +18 volt supply by the voltage drop across R231, R223.

The +5 volt supply, which is used for the logic functions is regulated by the voltage drop appearing across the +18 volt supply and R229.

The +7 volt reference supply is regulated by zener pack A1. The voltage to this circuit is fed by the +18 volt supply.

The +190 volt supply for the readout tubes is regulated by a voltage division which is referenced to the +18 volt supply.

B. Logic Section (Logic Schematic)

The Master Clock is a 33 Hz square wave generator and provides the timing for the entire instrument. The pulses from the flip-flop are fed to the clock input of a J-K flip-flop where the F and $\overline{F}$ pulses are generated. (Pictures A & B)

The F pulse is then applied to Q1 where the H pulse is generated. (Figure 3)

The 6 State Shift Register (Figures 3 & 6) are logic pack 4B generate the six timing pulses used for timing in the instrument. These are the $\overline{ZERO}$, A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, D, $\overline{D}$, E, and $\overline{E}$ pulses which are all clocked to the $\overline{H}$ pulses. This register is reset by the MS pulse from logic pack 16C at the end of each complete instrument cycle.

The 16 State Binary Counter (Figure 7) translates the pulses from the Current Controlled Oscillator into Binary Coded Decimal (BCD) output and controlls the Ladder Switches and the Decoder Driver. It is reset at the beginning of each time period by the $\overline{H}$ pulse.

The 9's Catcher operates gate 9B when $\overline{W}$ and $\overline{Z}$ and $\overline{A}$ to stop the Current Controlled Oscillator.

The Conditional 11's Catcher, logic packs 8A and 19B operate to stop the 16 State Binary Counter in the A period.

The 12's Catcher operates in the A period and causes the instrument to up-range and the Over light to turn on.

Current Controlled Oscillator produces a pulse train that is proportional in repitition rate to the current being supplied. The oscillator is stopped in F time. It's output is fed to the 16 State Binary Counter to be translated into BCD output. (Picture D)

Analog Cycle Control provides gating functions that prevent the instrument from recycling until it completes it's present cycle, thus avoiding erronious readings.

Display Circuits consist of the Function Lights, which are 5 volt lamps operated by the logic controls in the instrument and the relays and associated circuitry.

The Anode Strobing Control provides +190 volts to the readout tubes during the last half of each time period and lights each lamp in coordination with the proper time period.

Decoder Driver accepts the BCD output from the 16 State Binary Counter and translates it into decimal output, grounding the appropriate line to the readout tubes so that the tube will light when the +190 volts is applied by the Anode Strobing Control. Q41 operates the first readout tube whenever the count in A period reaches ten.

Manual Range Logic provides first priority of selection to the local front panel switches and provides the range commands as shown in Figure 8. Figure 9 shows the output as fed to the range flip-flop 18a and 18b.

Auto Range Logic operates when W and X from the 16 State Binary Counter and causes $\overline{UP}$ which initiates up ranging in the A period. $\overline{W}$ and $\overline{X}$ and $\overline{Y}$ and $\overline{Z}$ (zero) result in a $\overline{DN}$ signal which initiates down ranging in the A period. In addition when no Filter selection is made the instrument requires a settling time of about 10 ms. This is provided by R40 shunted by R41. When the Filter is selected R40 provides about 230 ms of delay for settling time.

IV. BUFFER BOARD THEORY

The buffer pre-amplifier of the 8300A is basically an inverting unity gain voltage follower. Its primary function is to provide an impedance conversion between the signal source being measured and the A-D Converter input.

Referring to Figure 16, the buffer could be represented as shown. The input resistance of the buffer is $\frac{E_s}{I_s}$ If I_s can be kept small, then the impedance will be high. The resistance R_L is the leakage resistance between the High and Low input termianls. Care was taken in the mechanical design of the instrument so that the leakage resistance would always be greater than 10^{12} ohms.

The other component of I_s is I_e. Elementary feedback theory indicates that the input resistance of an amplifier connected as shown in Figure 16 will be the product of the open loop input resistance and the loop gain. Junction Field Effect J-FETs, are used in the inputs of the buffer, and thus an open loop input resistance of greater than 10^9 ohms is obtained. The loop gain of the buffer is approximately 10^6, so the input resistance of the actual amplifier is greater than 10^{15} ohms, or much greater than the leakage resistance than could be expected at the input terminals.

Using J-FETs also helps keep the insertion current of the buffer preamplifier less than 50 pa. That means that a source resistance of 1 megohm would cause less than 50 μV or ½ digit of offset due to injection current.

The A-D converter has a full scale input of 12 volts, thus requiring a means of reducing input signals greater than 12 volts, if they are to be measured. For that purpose, a 10 megohm attenuator can be placed in front of the buffer when the input exceeds 12V.

The attenuator has two ratios available. One provides a division of 10 and the other provides a ratio of 100. Both are controlled by the front panel switches or the Remote Control Unit. In the 1000 volt range, the divider ratio is 1/100 and in the 100 volt range the ratio is 1/10. In the 10 volt range the input is direct.

The attenuator connection is as shown in Figure 17, with range commands adjacent to each switch. Limiting circuits are provided at the amplifier input, in series with current limiting resistors so that ±1100 volt signals cannot damage the buffer, even in the 10 volt range.

A zeroing circuit (R47) is provided on the buffer for calibration. The excellent zero stability of the FET pair used at the buffer input makes it unnecessary to provide front panel adjustment.

In addition to providing impedance buffering and signal attenuation, the buffer pre-amplifier also can be called upon to filter the input signal. Internal to the amplifier are roll off networks that establish a unity gain frequency of 3 Hz. This roll off of the gain of the buffer provides high frequency filtering by attenuating the AC signals inside the buffer and presenting a reduced version of the AC signal input to the A-D Converter. The frequency characteristics are shown in Figure 18. A notch filter is provided at 60 Hz and three pole response is present above 30 Hz. As the figure shows, for all frequencies above 50 Hz, the rejection of AC signal at the input is greater than 60 db.

Up to now the buffer has been considered as a single block amplifier. A more detailed explanation of circuit operation is in order. The block diagram shown in Figure 19 is complete enough for signal tracing. For illustration, place a positive DC voltage across the HI and LO input terminals.

Since AMP 1 is a high gain operational amplifier with its inverting terminal grounded, any signal at the non-inverting terminal will produce a large in -phase version of that signal at the amplifiers output. AMP 2 is connected inside of its own feedback loop to give a negative gain of about 2.5. When the amplified positive signal at the output of AMP 1 is applied to AMP 2's loop, the result is that the output of AMP 2 is driven negative. The voltage to which the output of AMP 2 is driven is determined solely by the input signal applied and the voltage to which the non-inverting input of AMP 1 is driven. Since the loop gain of the buffer is very high, the positive input of AMP 1 effectively does not change, and as pointed out earlier, the FET input does not allow any current flow from the source. Because there is no voltage present with respect to the analog common at the positive input of AMP 1, and because no current can flow from the source, the output of AMP 2 can only go to $-E_S$ with respect to analog common. Thus, we have an inverting voltage follower.

When FILTER is called with the 8300, large capacitors are placed in the feedback paths of both AMP 1 and AMP 2. In addition, both a notch filter and a low pass filter are placed in the forward gain path. The feedback capacitors force the 3 Hz unity gain bandwidth for the buffer, the notch filter provides 60 Hz filtering, and the low pass filter adds two additional poles at effectively 30 Hz.

V. AC CONVERTER THEORY

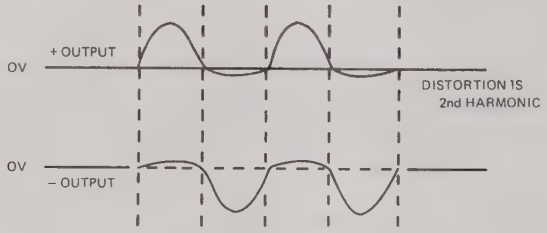
The AC Converter option for the 8300A converts input AC voltages, in four ranges, to DC for measurement by the A-D Converter. The output of the Converter is 0 to 12 VDC , which represents full scale.

Zero adjust for the AC Option is located on the Buffer Board and is accessable from the front panel. Calibration of the assembly is made in the factory prior to shipment and the board may be placed in an instrument, the zero adjustment made and calibration checked. It should not be necessary to recalibrate the option after installation.

The block daigram, (Figure 20) is divided into two major parts. A wide band operational re-

ctifier circuit where the ranging is accomplished and a DC difference (or subtracting) amplifier-intergrator where the rectifier output is filtered and amplified. The DC amplifier also provides the low source impedance required by the A-D Converter.

The operational rectifier circuit consists of an inverting transconductance amplifier and load resistor with feedback around them providing a loop gain of about 5×10^3 at mid band. The feedback is changed for ranging with reed relay switches. The input resistor is 1.11 megohms. This value shunted by the 10 megohm DC input divider is 1 megohm at the 8300A input. Q1 is a FET used as a source follower and Q2 provides a low impedance guard voltage which is used to bootstrap most of the capacity that otherwise would appear from the FET gate to common. The first two differential pairs are in a dual inline package. They and Q4 and Q5 develope the gain. Q3 and Q6 are current sources with such values that clipping due to overload is symmetrical. Changes in capacitor charges will be small and amplifier recovery time minimized. Q7 compensates for capacitance losses in the diodes at low levels. A symmetrical half wave rectifier placed between the amplifier and load resistor develops equal (+) and (—) DC voltages proportional to the amplifier output current. At full scale this current is near 2 mz. The two outputs have the following wave forms.



The DC difference amplifier-integrator filters the waveform and amplifies the DC difference between them by about 10 times for measurement by the A-D Converter. Three section filtering, which cannot be observed on the readout when the input voltage is at full scale and above 100 Hz. Below 100 Hz a few digits respond to the ripple. At 50 Hz the readout excursions do not exceed ±.01% of reading and at 30 Hz are within ±.05% of reading. Q9 is a dual FET which is used for the input of the low drift DC amplifier. Further gain for the DC amplifier is developed by a monolithic operational amplifier to produce a total loop gain at DC of about 5×10^5.

VI. MILLIVOLT/OHMS CONVERTER THEORY

As the name inplies, the Millivolt/Ohms Converter performs two functions. The use of the converter in the 8300A allows measurement of resistance over five ranges and provides two DC voltage ranges in addition to the three ranges offered by the basic instrument. The five resistance ranges are 1 KΩ, 10 KΩ, 100 KΩ, 1000 KΩ and 10 MΩ. The two additional DC voltage ranges are 1000 mv and 100 mv. As with the basic instrument, the above ranges have a 20% over-range capability. Thus the 1 KΩ range will accurately read to 1.19999 KΩ.

This converter can be thought of as two converters. One converter is a chopper amplifier which provides a DC amplification of an unknown voltage prior to A-D Conversion. Signal gain is necessary if a 100 mv signal on the 100 mv range is to provide a corresponding 10V DC signal into the A-D Converter.

The other converter in the Millivolt/Ohms Converter is a precision current ladder which, in conjunction with the Buffer amplifier, provides a known current through the resistor to be measured. Refering to Figure 21, a MOSFET chopper is used across the summing junctions of an operational amplifier. The signal developed due to the chopping action is amplified and presented through a capacitor to a half-wave synchronous demodulator. The Demodulator output is sent to a high gain (at DC) operational amplifier connected as an integrator. The integrator output is brought to the MOSFET chopper in a manner to insure negative feed-back. An input RC network provides input filtering to prevent beat frequency products at the amplifier output and balanced AC impedances for the chopper.

The use of the MOSFET chopper as shown allows the spike developed due to capacitive coupling from gate drive to channel to become a common mode signal for a high common mode rejection operational amplifier. Balanced AC impedances at the chopper provide cancellation effect of the offset current and voltage due to the capacitive spike. The new result is a chopper amplifier capable of operating at a fairly high frequency with small voltage and current offsets, and with spikes of low enough value to keep the AC amplifier from saturating. The above operation is achieved without large adjustments for spike compensation.

The overall millivolt amplifier can be considered to be a high DC gain operational amplifier utilizing potentiometric feedback to provide programmed gains of x10 or x100 and very high input impedance at DC. The A-D Converter follows the millivolt converter to provide digitization of the amplified analog representation of the input signal to the millivolt converter.

The current ladder is connected to the Buffer and the millivolt converter as shown in Figure 22. The inverting terminal of the Buffer amplifier is held very near analog common by the feedback connection of the unknown resistance. Because the inverting terminal is held near ground, and because the input current to the Buffer is small, the current through the unknown resistor is set by the reference voltage (7 volts) and the resistor selected by the range command. For the three upper KΩ ranges, the output of the buffer is presented to the A-D Converter. Thus since the A-D Converter digitizes 11.9999 as full scale, then that voltage must represent full scale on the KΩ ranges. Simple arithmetic shows us that the sampling currents for the three ranges to be 1 us, 10 ua, and 100 ua respectively.

For the 1 KΩ and the 10 KΩ range, smaller full scale voltages are used in order to keep load dissipation down. Thus, on these two ranges, the millivolt converter is used to amplify the voltage across the unknown resistor and present the amplified voltage to the A-D Converter.

In addition to providing smaller full scale impressed voltages in the lower two resistance ranges, the use of the millivolt converter allows a "modified four terminal" resistance measurement to be made. The term "modified four terminal" is used because the technique employed requires a small current in one of the sense lines that would not be present in a true four terminal resistance measurement. The sense current magnitude is determined by the voltage impressed on the resistor to be measured divided by R_i. By example, if the sense line resistance is 10Ω, then the error due to the sense current can be computed roughly as follows:

$$\text{Error} = \frac{10\Omega}{R_i} = \frac{100\Omega}{1000\Omega} = 10^{-4} \text{ or } 100 \text{ ppm of reading.}$$

If a two terminal reading were made at the 1 KΩ level with a 10Ω resistance in the hook-up wires, the error would be about 10,000 ppm. The improvement in performance using a "modified four terminal" measurement is obvious.

VII. EXTERNAL REFERENCE THEORY

The 8300A input terminal for VDC measurements is the input to the A-D Converter and therefore, will have a maximum voltage of ±12v with respect to the instrument common, Figure 23. Since it may be necessary to connect the common of the input to the common of External Reference input and the External Reference output common is instrument common, a means of isolating the commons becomes necessary.

Refer to Figure 24. Switches S1 and S2 are arranged so that when one set is closed, the other is open. S1 is closing during a non-critical (the A-D ZERO time) portion of the measurement cycle and allowed to charge to the voltage, E_R. When S2 is closed, the output of A_1 goes to E_R satisfying the voltage follower.

Refering to the circuit schematic, A2 is the S1 of the block diagram, Q4 and Q5 the switch, S2. A matched pair of J-FETS followed by a monolithic amplifier made up the high input impedance voltage follower. Q8 and R17 is a constant current source for the J-FET amplifiers. Frequency compensation is provided by the C4, C5 and C6.

The reference voltage is sensed through R18 from the A-D Amplifier board compensating for line drops. Low sense (Reference Common) also comes from the main board. CR7 and CR8 provide feedback to the voltage follower when the reed relay, S1 is open, keeping the amplifier output within 0.5v of the voltage of C8 to control the gate drive for Q4.

C7 forms an RC filter with the input driver giving improved noise performance. C9 provides an input impedance to the voltage follower during the time the FET switches, Q5 and Q6 are open.

Q1 and Q2 are gate drivers for the J-FET switches. Using the reference voltage for the collector supply of Q2 assures that the gate signal of Q4 never goes positive with respect to its terminal. The gate of Q5 is clamped to within .2v of common by diode CR6. R13 limits the current through CR6. C2 compensates for the capacity of CR6.

A voltage of as much as ±12.0v with respect to reference common will appear at the low terminal of EX REF input when the EX REF common is tied to the instrument input common.

A schematic showing the voltage distribution is shown in Figure 25. The MOS FET's used are P-channel enhancement mode devices. A negative gate voltage of 10v or more is needed to insure that the transistor is on. 0v or a positive gate voltage turns the transistor off. Refering to Figure 25, the upper switch needs a minimum of −15v to turn on and a maximum of 19v to turn off. The bottom switch needs a minimum of −22v to turn on and a maximum of 12v to turn off.

The MOS FET gate driver is redrawn in Figure 26 showing the peak voltages. When the transistor is saturated, CR1 is back biased. When the transistor is cutoff, C3 charges to 8v because of the 12v drop across the zener. This voltage subtracts from the collector voltage giving the voltage shown.

When the EXT REF control line is 5v (the EXT REF button pushed) −18v is applied to the local Disable line with Q10 and Q12.

Input protection is provided with CR4, CR5 and R12.

VIII. RECIRCULATING REMAINDER ANALOG TO DIGITAL CONVERSION (Figures 10, 11 and Schematics)

Refering to Figure 3 the time relationships can more easily be visualized. The Master clock generates a 333 Hz square wave, which is fed to the clock input of a J-K flip-flop, 3F, which produces the F and $\overline{F}$ pulses. The F pulse is further modified by Q1 where the H pulse is generated. The H pulses are fed to the clock inputs of the 6 State Shift Register, where five of the six timing pulses are generated. The sixth, $\overline{ZERO}$ pulse is generated by the action of the NAND gate 4B. Note that it is possible to divide any of the time periods into two equal parts by using the F and/or the $\overline{F}$ pulses. (These time periods are refered to as A1, A2, B1, B2 . . . etc.)

During the ZERO time period the $\overline{ZERO}$ pulse operates the A-D Auto Zero Drive Circuit. Q118 conducts and connects the output of A2 to the zero holding capacitor C115 and at the same time the input of the amplifier is grounded. This operation places the offset of A2 across C115 and effectively removes it for the remainder of the cycle. A similar circuit removes the offset from the Inverting Amplifier during "C" period of time.

For the purposes of illustration, it is necessary to make several assumptions and specify several conditions. The assumption is made that ranging functions are complete and that a voltage of –6.3524 volts is appearing at the input to the main chassis. (R102) The instrument is entering a Measurement Cycle.

The –6.3524 volts is amplified and inverted by the Inverting Amplifier and appears at the Polarity Detector which is enabled by Gate 4 pulse. The voltage is now positive due to the action of the Inverting Amplifier. The positive output to the Polarity Detector will cause the Polarity Detector to turn the plus gate Q112 on. This will cause the negative input to R102 to move directly to the input of the A-D Amplifier through R166. (In the case just taken the input to the instrument would have been positive. Had the input been negative, the Polarity Detector would have turned on the Minus gate, Q111 and the incoming signal would have been inverted by the Inverting Amplifier. This output is fed to the A-D Amplifier through R165.

NOTE: The inverting amplifier is used only when the input to the 8300A is negative.

The negative voltage appearing at the inverting input to the A-D Amplifier will cause a positive voltage to appear at its output. When the output of the A-D Amplifier exceed the 7.0 volt reference, the Analog Comparitor will produce current. This current is fed to the Current Controlled Oscillator (CCO). The Current Controlled Oscillator will produce a pulse train whose repitition rate is proportional to the current being supplied. These pulses are fed to the 16 State Binary Counter where they are translated into Binary Coded Decimal (BCD) output. The BCD output is connected to the Ladder Driver circuits and with each incremental increase of digit value the ladders will produce a current step. When the Primary Ladder has been caused to step 6 times the output from the Ladder being fed back to the input of the A-D Amplifier will cause the amplifier to satisfy itself with an output of less than 7 volts. At this time the Analog Comparitor will no longer supply current to the Current Controlled Oscillator and no further pulses will be generated. The remainder voltage that appeared at the output of the A-D Amplifier to satisfy it is now applied to capacitor C118 through Q125 which was enabled by the Gate 2 pulse (Sample and Hold)

The secondary Ladder output is fed to capacitor C110 in Display Storage. The BCD output of the 16 State Binary Counter is also fed to the Decoder Driver, where it is decimalized, which will cause ground potential to appear on the "6" line to all readout tubes. The A pulse and the

F pulse are fed into the Anode Strobing Control which will cause the +190 volts to be pulsed on during the last half of the A time period, thus causing the "6" to be displayed by the first readout tube.

At the beginning of the B time period the $\overline{H}$ pulse will reset the 16 State Binary Counter. The Gate 1 & 22 pulse will enable Sample and Hold transistors Q124 and Q127. The remainder voltage stored on capacitor C108 is now applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and again the Analog Comparitor will produce current, which is fed to the Current Controlled Oscillator. The oscillator pulses are counted by the 16 State Binary Counter and converted to BCD. The Ladders are caused to increase their output incrimentally with each pulse until the Primary Ladder feeds a "3" pulse back to the summing junction of the A-D Amplifier. At this time the output of the amplifier is less than 7 volts which causes the Analog Comparitor to stop the current flow to the Current Controlled Oscillator. Etc. The remainder voltage appearing at the output of the A-D Amplifier is applied to capacitor C109 in the Sample and Hold circuit through Q127. The Secondary Ladder output is stored on Display Storage capacitor C111 through Q129 and Q147.

Again the Decoder Driver has caused a ground potential to appear on all of the "3" lines to the Readout tubes and the F pulse through CR105 and the B pulse through Q34 will cause the +190 volts to be applied to the second readout tube, where the digit "3" will be displayed.

The process continues using alternately capacitors C108 and C109 in the Sample and Hold circuit to store the remainders and then reapply them to the summing junction of the A-D Amplifier. As each time period digit is developed, the Secondary Ladder stores its output on seccessive capacitors in the Display Storage capacitors C110 through C114.

It is well to remember that the above description was of a Measure Cycle. All of the digits were developed using the Sample and Hold circuit. The following description is of the Storage Cycle.

Gate pulse 4 is the primary control over the determination of whether the 8300A will enter a Measure Cycle or a Storage Cycle. If Gate 4 pulse is not present the Polarity Detector will not be activated and the instrument will continue in Storage Cycle. Gate 4 pulse is generated by Q116 and will only be present in A period when an M signal is present.

Since in this example we are entering a Storage cycle no Gate 4 signal will be present and Q146 in the Display storage will be enabled. The last Measurement Cycle left incremental voltages stored in the Display Storage capacitors C110 through C114 that correspond to the digits 63524.

During the A period Q128 and Q146 will be enabled allowing the voltage stored in C110 to be applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and the Analog Comparitor will supply current to the Current Controlled Oscillator. The oscillator will generate a series of pulses causing the 16 State Binary Counter to translate the pulses into BCD output. The BCD output will cause the Ladders to switch until the Primary Ladder output satisfies the A-D Amplifier feedback. At this point in time the output from the amplifier will be below 7 volts and the Analog Comparitor will no longer supply current to the CCO. The pulses stop and the output of the Secondary Ladder will again be stored in capacitor C110 in the Display Storage circuit. The BCD 6 from the 1 6 State Binary Counter will drive the Decoder Driver which will produce a ground potential on all of the "6" leads to the readout tubes. The combination of A and F pulses will cause Q35 and Q40 to apply +190 volts to the anode of V1 which will light the "6".

During the B period, Q129 and Q147 will be enabled, applying the voltage stored in C111 to be applied to the summing junction of the A-D Amplifier. The output of the A-D Amplifier will

exceed the 7.0 volt reference and the analog comparitor will supply current to the Current Controlled Oscillator. The pulses from the CCO will be counted and translated to BCD output by the 16 State Binary Counter.

The BCD output being applied to the Ladder Driver Circuits will cause the ladders to increase their outputs until the output of the Primary Ladder, which is fed back to the summing junction of the A-D Amplifier satisfies the amplifier. At this point in time the output of the amplifier will be below the 7.0 volt reference and the Analog Comparitor will no longer furnish current to the CCO and the pulses will stop. Since a "3" was digitized and stored in the Display Storage for this time period, a three from the Primary Ladder will cause the A-D Amplifier to be satisfied. The output of the Secondary Ladder will be stored in the Display Storage during the last half of the time period and the "3" will be displayed by V2 during the last half of the time period by the operation of the Anode Strobing Control.

Each increment of voltage stored in the Display Storage will be digitized and re-stored in the Display Storage circuit until all five digits have been displayed. At the end of the Storage Cycle if no Measure pulse has been generated prior to A time the 8300A will again enter a Storage Cycle. This process will repeat until a Measure pulse is generated, prior to A time and then at A time a Gate 4 pulse will be generated and the instrument will again sample the input voltage and enter a Measurement Cycle.

IX. TROUBLESHOOTING AND ANALYSIS

1. The following is a list of recommended test equipment that is required to test and calibrate the 8300A. If the recommended equipment is not available, other equipment which meets the required specifications may be used.

EQUIPMENT NOMENCLATURE	RECOMMENDED EQUIPMENT
Oscilloscope	Tektronix Model 547
Oscilloscope Plug-In	Tektronix Model 1A1
Oscilloscope Probes	Tektronix Model P6010
DC Voltage Source	Fluke Model 343A DC Voltage Calibrator
AC Voltage Source	HP Model 745A
Differential Voltmeter	Fluke Model 885A

2. An excellent source of synchronization for the Oscilloscope may be obtained by using the $\overline{\text{ZERO}}$ signal that is available at TP4 or TP108. By proper adjustment of the horizontal trace time it is possible to see all of the other timing pulses in their proper relationship.
3. With the covers and shields removed it is reasonable to expect to see more noise in the output as the 8300A is quite sensitive to interference when these protections are removed.
4. Figure 30 gives the general location of the various sections of the instrument.
5. Figure 29 locates the various test points (TP) and is a guide to the location and index of the logic packs.
6. All voltage measurements and pulse observations should be made with reference to the instrument signal ground which is available at TP3 and TP109.
7. Figure 27 gives a step by step procedure for troubleshooting the Display section of the 8300A.
8. Figure 28 gives an excellent step by step procedure for troubleshooting the analog circuitry.
9. Many cases of trouble can be analized from the operation and readout observations of the instrument. As examples the following are presented:

   a. Readout is in error only in the negative polarity.

      It is reasonable to assume that the trouble is located in either the polarity FET switch-or in the Inverting Amplifier since these paths are utilized only in the negative polarity.

   b. More than one digit displayed in the readout tubes.

      The Decoder Driver is the most likely source of this trouble. If ground potential is supplied to more than one of the decimal lines to the readout tubes, multiple numbers will light. There remains the possibility that the Anode Strobing circuits are mal-functioning.

c. Only the first digit is displayed, all others read 0.

It is reasonable to assume that the remainders are not being stored in the Sample and Hold circuitry. This can be caused by a failure in the FET switches or a short in the storage capacitors. It is also possible that two significant digits will be developed and displayed.

d. First digit reads higher than the input voltage and all other digits read 0.

Count the pulses from the Current Controlled Oscillator. If correct check the BCD output of the A4 Counter. If the BCD output is correct the Ladder output voltage could be too high.

e. A large signal of either polarity is needed to cause a reading of other than 0.0000.

The A-D Auto Zeroing circuit, Q117 and Q118 should be checked.

f. None of the readout tubes lighted.

Check the +5 and the +190 volt supplied.

10. The basic instrument may be checked by applying a 0 to 12 volt DC signal at the input to the Inverting Amplifier. This should cause the instrument to display the voltage applied.

11. By applying a jumper between TP6 and TP201 the instrument can be made to sample continuiously. This procedure can be used to locate trouble in the Storage circuitry.

12. The logic section of the instrument can be broken up into several independent sections for trouble analysis as follows:

a. Master Clock

Check the output of Q45, then look for the F, $\overline{H}$ and $\overline{ZERO}$ pulses.

b. Six State Shift Register.

Check for the presence of the A, B, C, D, and E pulses and their inversions.

c. Check the output of the Current Controlled Oscillator and the BCD output of the 16 State Binary Counter.

d. Display readout tubes.

Anodes and Anode Strobing circuitry.
Cathode circuits including the Decoder Driver.
Decimal lines.

e. Function Indicators.

+5 volt incandescent lights and associated circuitry.

f. Sample Oscillator should be checked for output.

g. Figures C through G and the Picture waveforms attached will be of additional assistance in locating troubles.

X. DATA OUTPUT UNIT

The Data Output Unit Option is felt to be included in a minority of cases, this section will include the theory of operation and the troubleshooting and analysis.

A. General

The Data Output Unit (DOU) receives DVM measurement data through guarded pulse transformers and by means of appropriate control circuitry, enters this data into a self-contained, random access digital memory. Outputs are available in positive logic, BCD 1-2-4-8 parallel format. A strobing operation, which produces a parallel bit, serial-character format may be easily implimented by connecting outputs together in groups, as desired, and manipulating gate inputs. (See DOU Block Diagram, Figure 40)

A system of output blanking is incorporated which has a threefold purpose. First, it holds all outputs in an OFF state any time the DVM is performing a measurement or is in the digitizing process. It is during these periods that the DOU memory is being loaded and if the outputs were turned on, transient, meaningless data would be momentarily displayed. Secondly, signal conditioner settling time is automatically considered by a circuit called the Programmed One-Shot (POS). The POS ensures that the user obtains rated accuracy data in the minimum possible time, reguardless of the function performed, by holding outputs off or blanked until valid data is obtainable. The POS holds outputs OFF just long enough for the signal conditioner in use to settle to rated accuracy. When a different signal conditioner is called into operation by the user, the POS automatically adjusts timeout delay to the new conditions. At timeout, the POS triggers a new measurement before turning on the outputs 23 milliseconds later. Thirdly, automatic ranging is detected by the DOU, and data outputs are blanked during ranging functions. After blanking is complete, the outputs will remain ON and unchanged until the DVM is again commanded to sample.

The following is an example of a typical sequence of internal events as initiated by the user generated sample command:

a. An unknown input and a trigger pulse (command to sample) are applied to the DVM.

b. The POS reverts to its unstable state, thereby inhibiting all outputs.

c. The DVM makes a preliminary measurement (requiring 6 milliseconds) to determine if ranging is necessary.

d. Autoranging takes place and the timeout is increased by 250 milliseconds for each range change.

e. The programmed one-shot begins to time out in accordance with the function delay data registered in the DOU memory.

f. At the end of the required settling time, the DVM is automatically commanded to sample again by the POS as it reverts to its stable state.

g. New data is registered in the DOU memory as a result of this final sample.

h. All the outputs are then turned ON to provide function, range, polarity and the specified accuracy numerical data. A ready flag indicates whether outputs are on or off.

B. Logic Notation

A description of the logic symbology used in the DOU is given in Figure 40. A J-K flip-flop that is in the "1" condition or is set "high" has a high output from the Q terminal.

The orientation of the flip-flops in the schematics is the same as the flip-flop shown in Figure 40.. This method of notation enables input/output terminals of the flip-flops to be identified without the necessity of redundant lettering of each device symbol. In the main, the routing of logic and control signal on the schematics is accomplished without connecting lines, which greatly reduces conjestion. The routing of the memory outputs within the DOU is given by numerical designations. For example, 16-P3, which appears at pin 2 of output buffer gate 3A, refers to pin 3 of shift register 16.

C. Multiplexers

The DVM function, range and polarity inputs are applied to dual multiplexer circuitry consisting of transistors Q14 through Q20 and NAND gates 28A, 28B and 28D (see DOU schematic). The five gates comprising each multiplexer are enabled sequentially by the 6 State Shift Register signals. The multiplexer outputs are applied to trigger circuits consisting of NOR gates 27A through 27D and transformers T1 and T2. The pulses produced by T1 and T2 secondaries are applied to RS flip-flops composed of inverters 13B. 13C, 13E and 13F which reconstruct the multiplexer inputs for application to the data gates. Examples of the RS flip-flop outputs are shown in the timing diagram of Figure 41. (Signals (9) and (10)) and correspond to the following DVM functions and input conditions: VDC function with filter, 100 range and positive voltage applied to the input. A complete list of waveforms appearing at the output of the RS flip-flops is given in the troubleshooting section of the manual.

D. Digits Counter

The digits counter consists of J-K flip-flops 26W, 26X, 25Y and 25Z. The input flip-flop 25Z is toggled by positive pulses, which are transferred through the guard by transistor Q13 and transformer T3. The counter produces a 4 bit binary output that is entered into the memory via the data gates. The counter is reset at the beginning of each su-period of the measurement cycle by the $\overline{F}$ signal. The W', Y', and Z' counter outputs are also applied to NAND gate 22A, which stops the counter at a count of "11" and generates a high at the input of flip-flop 21L. If another pulse appears at the secondary of T3, it is indicative of "12" in the first decade (i.e. instrument overload). The 12th pulse toggles flip-flop 21L to produce an overload indication at the DOU output, pin 35B.

E. Data Gates

The data gates consist of NAND gates 22B, 23A through 23C and 24A through 24D. The gates are controlled by F', F', S and S signals so that the 10 bits function, range and polarity data and 20 bits of numerical data are presented to the shift register memory at the proper times. These data bits are loaded in accordance with the load sequence. (Figure 42) and are steered by these data gates.

F. Random Access Memory

The DOU memory is composed of shift registers 10, 12, 14 and 16. Data is loaded serially into the shift registers. The loading sequence is controlled by clock pulses, which are produced by gates 15A through 15D, gate 19D and associated circuitry. Steering signals S and S together with the loading signal F', develop loading pulses as shown in Figure 43. NAND gate 19D inverter 13A and associated circuitry delay the F' signal for approximately 10 microseconds so that all data present at the shift register inputs will be stabelized before clocking occurs.

G. **Control**

F′ and $\overline{F'}$ signals are produced by an RF flip-flop consisting of NOR gates 19A, 19B and associated circuitry. The trigger for the flip-flop is developed by gates 29A through 29C and transformer T4. The F′ and $\overline{F'}$ signals are conditioned by the $\overline{F}$. $\overline{M}$ and $\overline{ZERO}$ signals so that the F′ and $\overline{F}'$ signals occur only during periods A through E of the DVM measurement cycle. The steering flip-flop is triggered by the F′ signal and produces S and $\overline{S}$ signals.

The $\overline{S}$ output of the steering flip-flop is applied to transistor Q9 and associated components, which comprise a rechargable one-shot. This circuit is responsible for initializing control circuit conditions and providing for generation of the M signal. The sequence of operation of the one-shot and associated circuitry is as follows: (Control timing signals are shown in Figure 43.)

a. Measurement cycle is initiated.

b. RS flip-flop 19A, 19B are set to "1" condition. (Pin 2 of 19A high)

c. Flip-flop 20B is reset by $\overline{F}'$.

d. Overload flip-flop 21L is reset by a measurement inclusion signal generated at pin 9 of flip-flop 20B.

e. Measure/Store flip-flop (20A) is set by overload reset signal. (Signal No. 4)

f. Gate 17C is inhibited, thereby inhibiting all output buffer gates.

g. The steering flip-flop is toggled (middle of "A" period) and capacitor C14 begins to charge toward +5v.

h. The steering flip-flop is again toggled (middle of "B" period) and capacitor C14 is quickly discharged to 0.9v.

i. Steps (f) and (g) repeat for "C", "D" and "E" periods.

j. Following "E" period, C14 continues to charge until Q9 tis turned on.

k. Q8 then turns on and sets the overload reset flip-flop (20B) and the steering flip-flop (21S).

l. The Measure/Store flip-flop is reset by a negative trigger developed in the circuit of Q7.

m. The output buffer gates are enabled and the data becomes available.

In addition to providing a pesudo Measure/Store signal, the circuit of flip-flop 20A and transistor Q7 also function as an autorange detector Control signal timing under autorange conditions is shown in Figure 43.. If the decision to autorange is made, (middle of "A" period), the DVM logic places the instrument in storage mode. This locks out the F signal in the DOU control circuit and, consequently, no pulses are produced in T4 secondary, excepting the first. With no F′ signal to toggle filp-flop 21S, the rechargable one-shot times out and sets the overload reset flip-flop to the "1" condition. The resulting signal (signal N.2) is applied as a reset pulse to Q7, however, because capacitor C15 has not had time to discharge sufficiently, the trigger threshold of flip-flop 20A is not reached and the flip-flop remains in its previous state. Thus, the output buffer gates are inhibited during the autorange operation. If the instrument had not autoranged, C14 would have acquired sufficient charge during the measurement cycle to enable flip-flop 20A to be triggered, as shown in the timing diagram of Figure 43.

The programmed one-shot consists of NOR gates 18A and 18B, transistors Q3 through Q6, capacitors C9 and associated programming resistors. In its stable state, gate 18A output is high and gate 18B is low. Assume that an external trigger is applied to pin 34 of connector B. The trigger enables gate 18C, thereby triggering the DVM to initiate a measurement cycle. The trigger also enables gate 18A, and the POS then switches to its unstable state. When the POS switches states, the output of gate 19C goes low, resulting in gates 17C being inhibited, Inhibiting gate 17C causes all of the output data buffer gates to be inhibited.

The timeout of POS delay is initiated as soon as the circuit is triggered, i.e., when the POS is triggered, switch Q3 is turned off and C9 begins to charge through the programming network to +5 volts. Delay time is controlled by the memory, which selects resistor R19, R20, R21 or R22, depending on the selected DVM function. When C9 has accumulated sufficient charge, transistors Q4 and Q5 are connected to operate like an SCR, turn on, applying a positive pulse to the input gate 18B through capacitor C24. The POS switches back to its stable state and retriggers the DVM for a final measurement.

The POS is automatically retriggered if the DVM autoranges as a result of the final measurement. For example, if a step voltage were applied to the DVM in mvDC mode, the DVM[logic might not make an autorange decision before the measurement caused by POS to time out. If this occurs, NOR gate 18C goes high, retriggering the POS and initiating a second delay. All autorange operations that are to occur do so at this time. Termination of the second POS delay causes yet another measurement. All settling times have been considered at this time, this measurement is the last and upon completion, 23 milliseconds later, outputs are turned on and data becomes available.

In VDC mode without the FILTER function called, transistor Q6 is enabled. This programs the POS for fastest timeout and clamps pin 9 of gate 18D so that the DVM will not be retriggered by POS timeout.

DATA OUTPUT UNIT TROUBLE ANALYSIS

Trouble analysis of the Data Output Unit is most effeciently performed by a systematic sequence through the unit beginning at the malfunctioning output(s) and working progressively backwards. As familiarity with the unit increases the operator will discover he can shorten the process by skipping obviouse irrelevant steps.

In any analysis certain decisions and/or conclusions must be made. Consult Figure "A" for the suggested decision sequence. Figure "B" is a table which should help to determine how to make the decisions.

FIGURE""B" DECISION AIDS

Example No. 1 DOU Outputs or Reader Faulty?

This decision must be based upon a point-by-point measurement of DOU outputs at points of origin. Many short-cuts are available depending upon the nature of the reader. Suppose all decades except the third are producing correct numbers. The third decade generates the following table:

8300 PANEL	READER PANEL	
00000	00400	CONSIDER: An open in the cable from the DOU to the reader (probably pin 26B DOU connector.) This is the "4" line of the 1-2-4-8 four line BCD code.
11111	11511	
22222	22622	
33333	33733	
44444	44444	
55555	55555	
66666	66666	
77777	77777	
88888	88288	
99999	99399	

Example No. 2

8300 PANEL	READER PANEL	
00000	08000	CONSIDER: An open DOU to reader (probably pin 9A DOU output connector.)
11111	19111	
22222	21222	
44444	42444	
88888	88888	

Example No. 3 Reader panel is 155555, DC+, MV, AC, K, M, EX REF, FLT

The above display remaining regardless of 8300 panel.

Check: Pin 32B DOU Connector. If not 0 to 0.5 VDC, disconnect reader and measure again. If now 0 to 0.5 VDC, reader is at fault, if not look for the problem in the DOU circuit.

NOTE: The forgoing examples assume a reader with full overranging in each decade. Other overrange patterns will not defeat the analysis if the pattern is known.

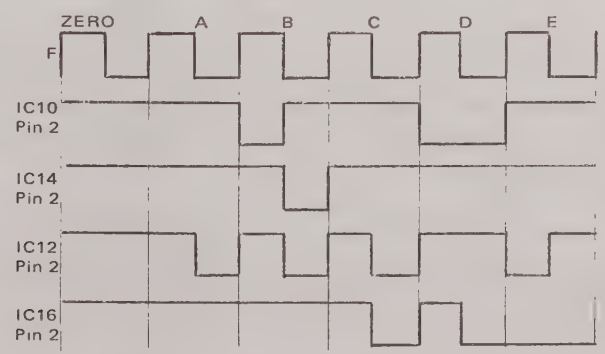
Example No. 4 DOU Memory contains correct data?

It is assumed here that data outputs were determined faulty. This is a static test. Set the 8300 stimulious to produce the trouble analysis information desired. Command to sample once and no more. Using a VTVM, check the data in shift registers (DOU memory) 10, 12, 14, and 16. Use chart of Figure X-4 for location of data. All data in this memory is inverted phase (e.g. 6 would normally be 0110; it is in the memory as 1001.) The chart of Figure X-4 will prove to be a valuable tool for several areas of the DOU circuit.

If the data in the memory is correct, the problem must be in an output buffer gate or in the 1st decade binary to BCD converter I/C 11. If not, it must be determined whether a shift register is faulty. This is proven by determining that serial data input signals are correct and that load signals are correct.

Example No. 5 DOU Memory input data correct?

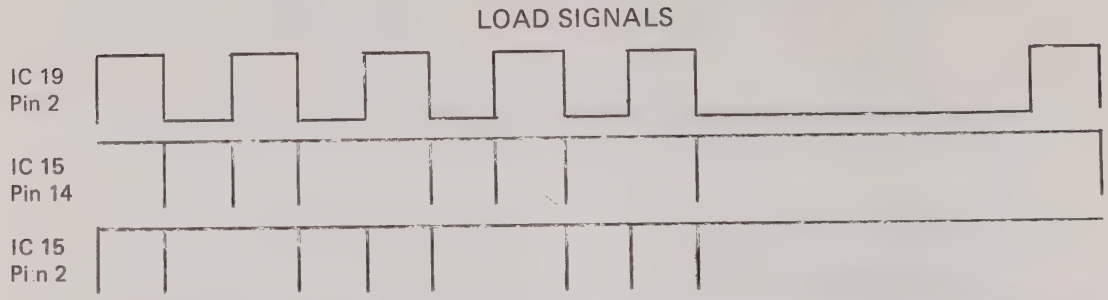
Unfortunately, this must be determined with a dynamic test and for the uninitiated may require observation of a properly operating unit. Set stimulous equipment (8300 & input source) for desired trouble analysis information. Set internal sample command pot on the 8300 to ext position and externally trigger the instrument. The rate should be 25 pps for good scope displays. Ignore reader display as it is unimportant at this time. Sync the scope with the F signal and observe shift register data inputs. Refer to the wave-shape index (Figure "D" reference point no. 9) and index (Figure "E" reference point no. 10). These waveforms are multiplexed with numerical data from the counter and inverted by registration gates I/C 22, 23, 24. Study the schematic and Figures X-4, D, and E to visualize what appearance these signals should have for various combinations of data. A table is not given as there would be 256 possible patterns. It is easier to figure out what a particular combination should produce and will require only a few seconds for an experienced operator using Figure 43. Again remember the inverted phase.



Example: 26.391 VDC FILTERED

Example No. 6 DOU load commands correct?

Refer to the figure below. Use the same set-up as in Example No. 5. A dual trace scope is useful.



If the load commands are correct then something may be wrong with the operation of one of the shift registers. It should be considered (if replacement does not solve the problem) that one of the shift register outputs may be shorted.

Example No. 7 Are the multiplier outputs correct?

Use the same set-up as in Example No. 5. Figures "D" and "E" give tables which illustrate all possible waveforms at I/C 3 Pin 6 and I/C 13 Pin 10 respectively. If the waveforms are correct registration gates I/C 22, 23, 24 may be faulty.

Example No. 8 Are counter jumpers installed?

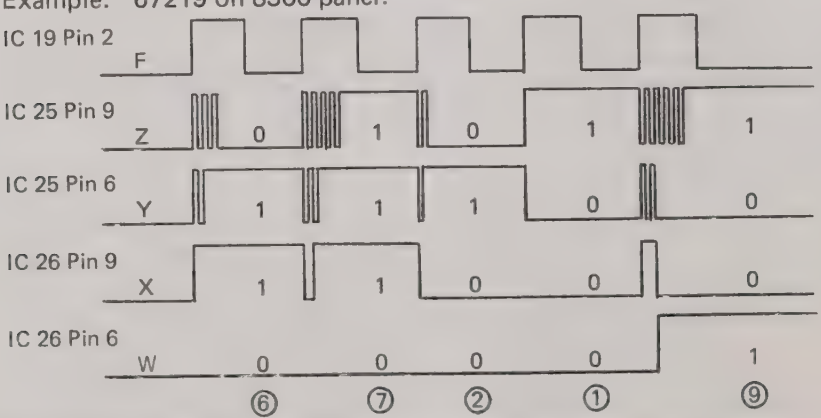
With the reader connected, check continually between the following points:

23A and 3A 20A and 4A 21A and 1A 22A and 2A	DOU OUTPUT CONNECTOR	IC 25 pin 9 & IC 24 pin 13 IC 25 pin 6 & IC 24 pin 1 IC 26 pin 9 & IC 24 pin 4 IC 26 pin 6 & IC 24 pin 10	Convenient Alternate Locations

Example No. 9 Are the counter outputs correct?

Use the same set-up as in Example No. 5. Consider counter outputs only during second half of each subperiod as below:

Example: 67219 on 8300 panel:

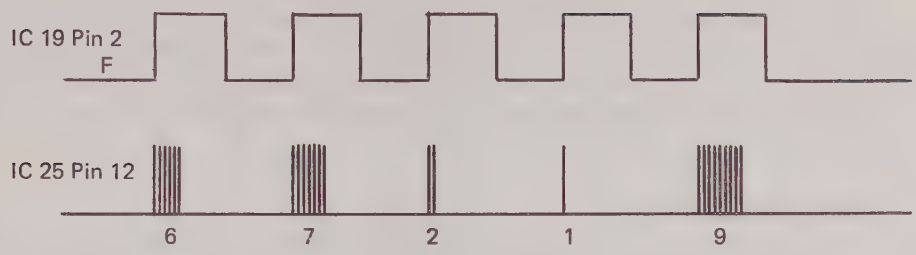


Again, correct counter operation is indicative of a problem in registration gates IC's 22, 23, 24.

Example No. 10 Is counter input correct?

Use the same set-up as in Example No. 5.

Example: 62719



Correct input but incorrect outputs are indicative of counter malfunction.

Example No. 11 Are signals correct at I/C No. 27 pins 3 and 13?

DOU circuit is inside the guard. Therefore the scope must be synced on a signal inside the guard. Use $\overline{\text{ZERO}}$ signal at TP 4 and Common TP3. If multiplexer outputs (test of example 7) are incorrect but observations of example 11 are normal, the transformer circuits of T1 or T2 may be faulty. Signals at pins 3 and 13 of I/C 27 should have waveforms like figures D and E respectively. If not, multiplexers may be at fault or wires broken between DOU input terminals and the counnector inside the guard box.

Example No. 12 Data, Ready or Overload problem?

This is a static test. Command the 8300 to sample only once and then observe, Rate pot on front panel is in external position. If numerals range, polarity or function data is faulty it will be observed on the reader (monitor). If the reader is either blank or displaying 1555.55 VDC+, FILT, MV AC, KΩ, MΩ, EX REF., then the ready line is probably high. The overload display should coincide with a numeral display of 119999 and will be visable on the reader.

Example No. 13 M or P.O.S. problem?

Command to sample only once. Rate pot on the front panel should be in the external position. Check I/C 19 Pin 12 for 0 to 0.5v (P.O.S.) and I/C 17 Pin 17 for 3.5 to 4.5v ($\overline{\text{M}}$ signal). If the $\overline{\text{M}}$ is low it is likely that P.O.S. will be high, but the cause will be $\overline{\text{M}}$ from the control circuit; If $\overline{\text{M}}$ is normal but P.O.S. is high, the programmed one-shot is faulty.

Example No. 14 Are P.O.S. jumpers installed?

Visually check to insure that jumpers 1 & 2 are installed or jumper 1 or 2 and R50 in accordance with delay length table. This is a factory installation so this part of the trouble analysis procedure applies only to factory check-out.

XI. REMOTE CONTROL UNIT

A. General

The RCU functional block diagram is given in Figure 44. . The input function and range commands are applied to circuitry which provides logical interlocking, so that the RCU will respond only to acceptable command combinations. The range and function commands are applied to the photodetectors inside the guard chassis via the light emitting diodes (LED's). The resulting signal is applied to the switches, which activate the DVM control lines.

B. Circuit Description

Input functions and range commands, consisting of switch closures or zero volts DC, are applied to the inverters. The inverter outputs are applied to NAND gates, which provide logic interlocking and drive the light emitting diodes, CR1 through CR11.

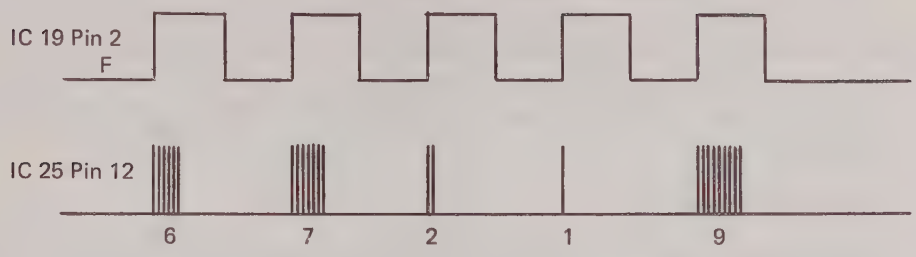
The logical interlocking is such that the instrument will respond to the first call received and will ignore succeeding erroneous calls until the first call is released. For example; if KΩ function were called, gate 7B would be enabled, which would inhibit gates 4A, 7A, 3A, 3B and 4B, thereby preventing EXT REF, VDC, MVDC, VAC and 10 MΩ functions from being called.

The detector circuitry consists of phototransistors Q1 through Q11, which detect and amplify the LED outputs. The output of the phototransistors is applied to the output switches and their drivers, transistors Q12 through Q29. The phototransistors and switches are enabled by the remote function and remote range busses, which supply +5 volts DC to the circuitry when the remote switches are pressed.

Example No. 10 Is counter input correct?

Use the same set-up as in Example No. 5.

Example: 62719



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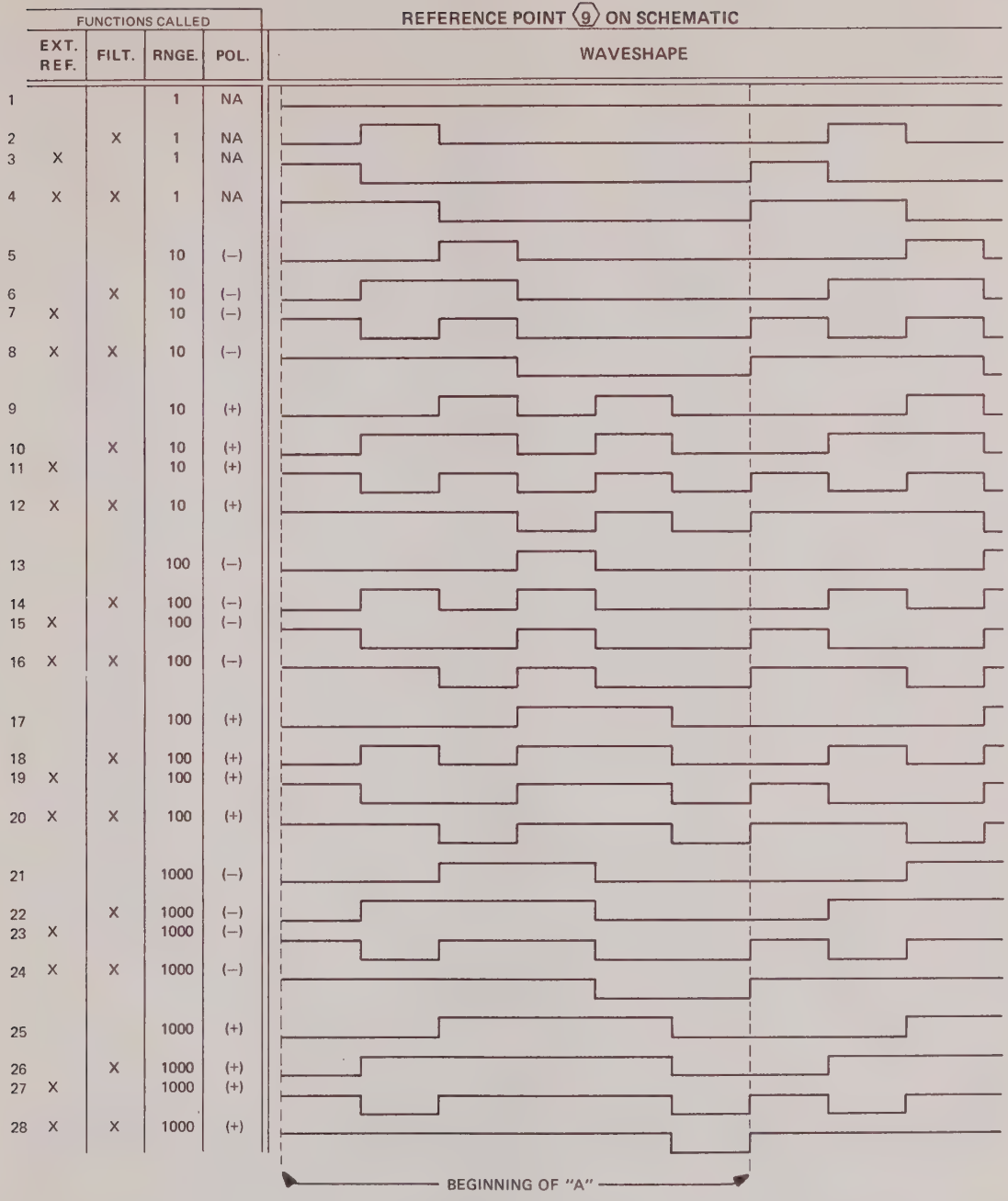


Figure "D"

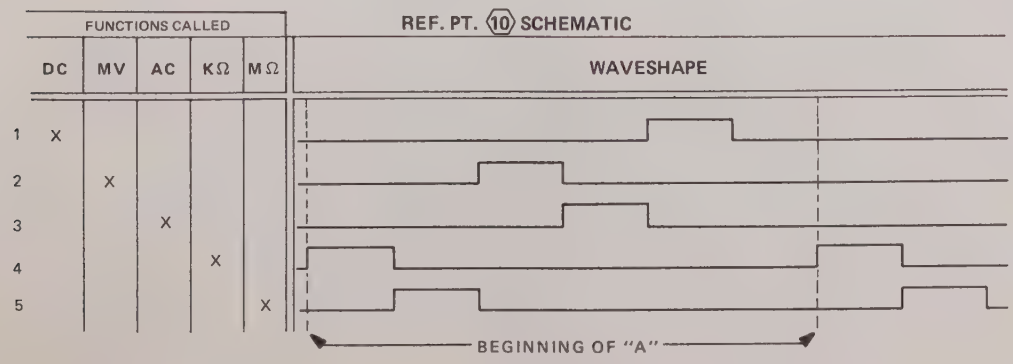


Figure "E"

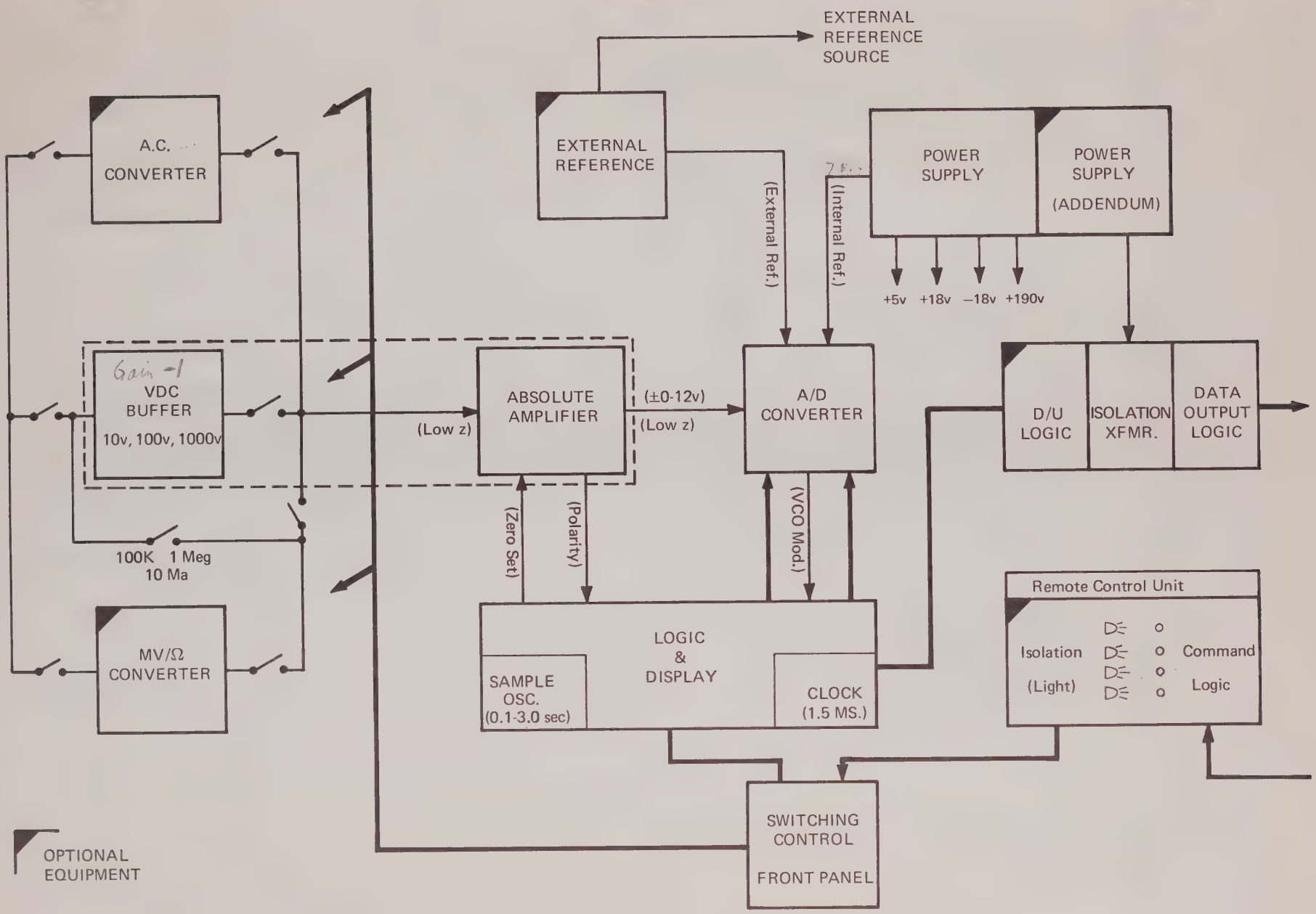


Figure 1. BASIC BLOCK DIAGRAM

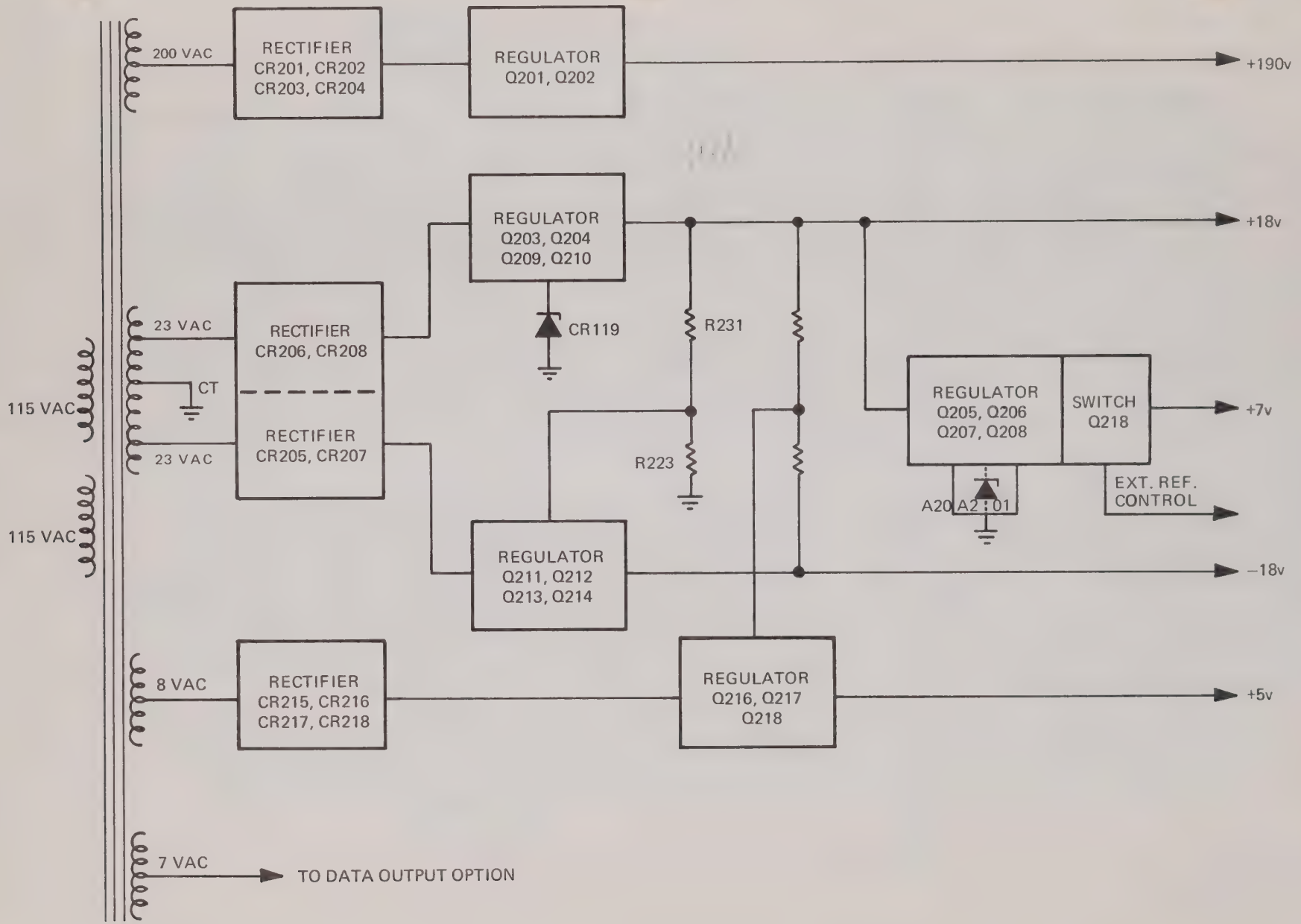


Figure 2. 8300A POWER SUPPLY

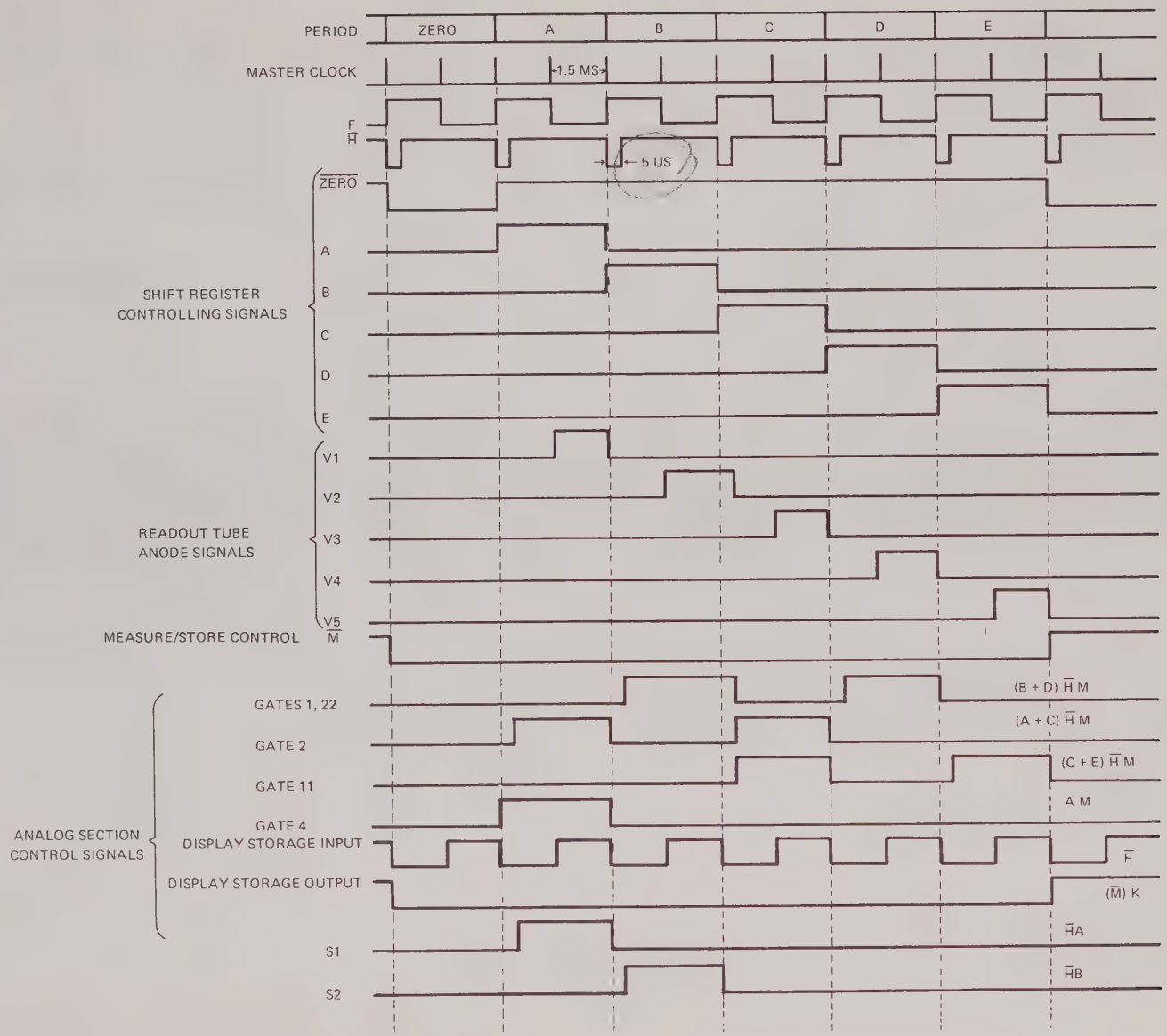


Figure 3. MEASUREMENT CYCLE TIME RELATIONS

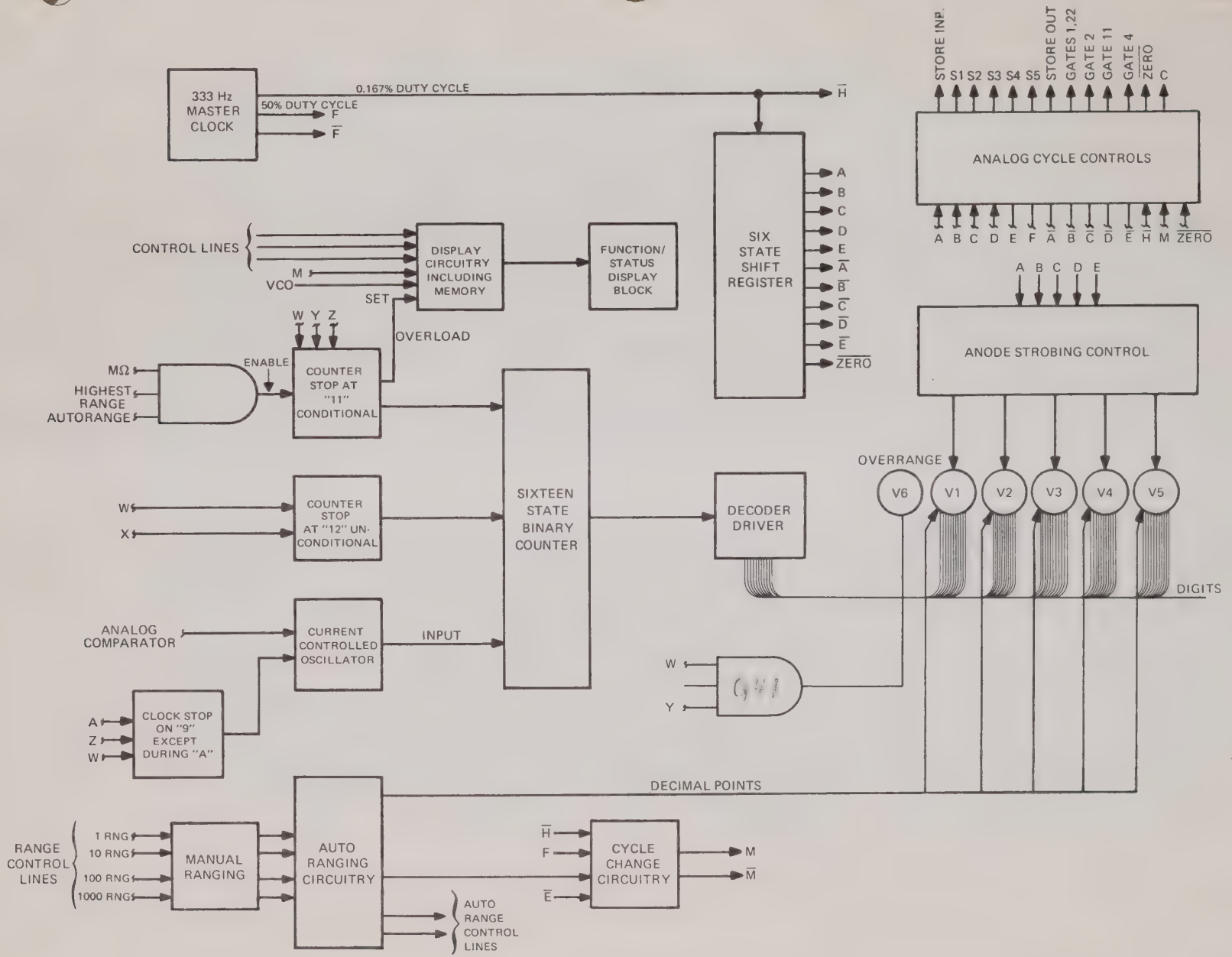


Figure 4. DVM LOGIC AND CONTROL

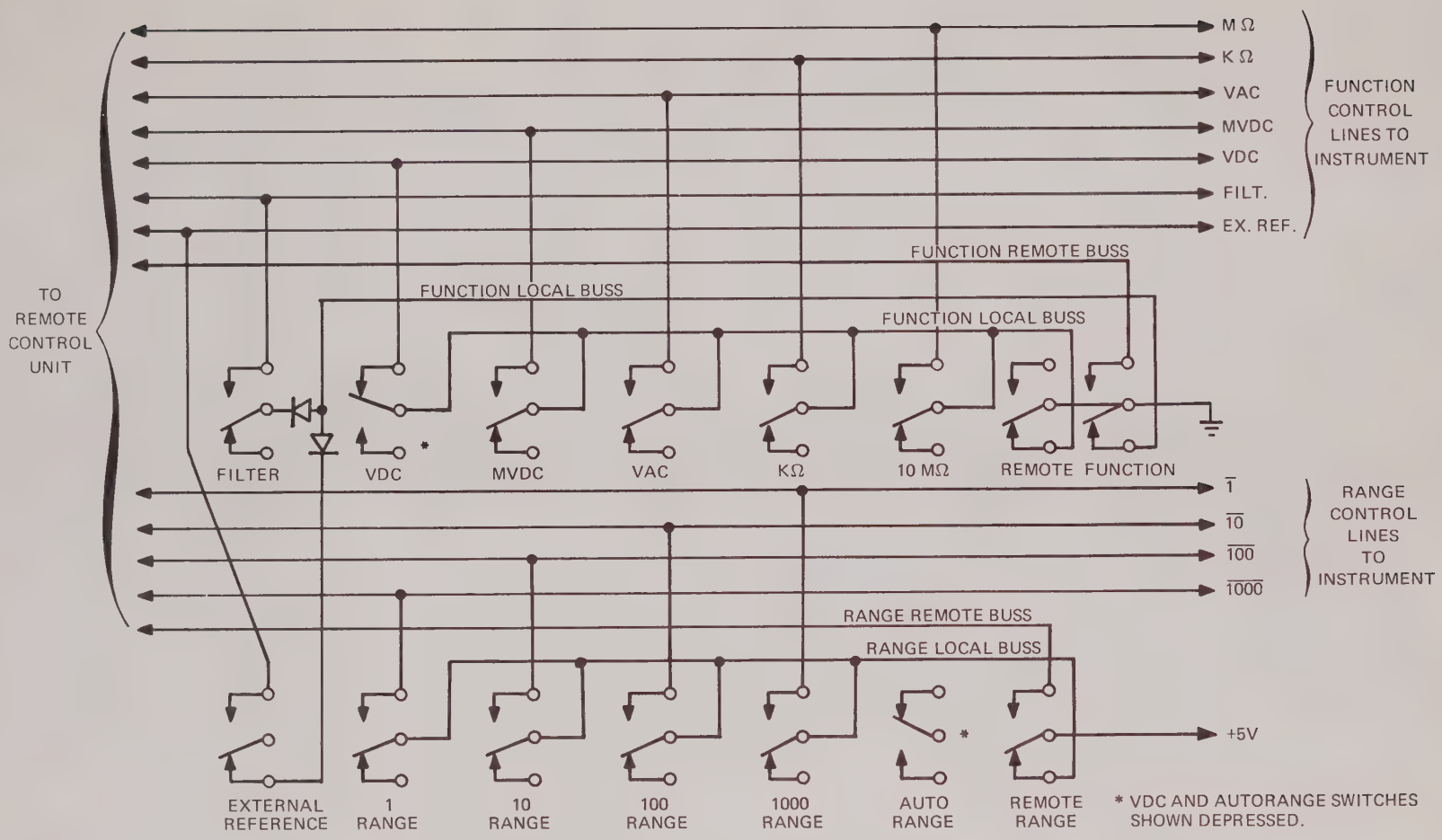


Figure 5. CONTROL SWITCHING

PERIOD	SIX STATE SHIFT REGISTER				
	1A	1B	2C	2D	3E
ZERO	0	0	0	0	0
A	1	0	0	0	0
B	0	1	0	0	0
C	0	0	1	0	0
D	0	0	0	1	0
E	0	0	0	0	1

Figure 6

CCO PULSE COUNT	16 STATE BINARY COUNTER			
	7W	7X	6Y	6Z
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0

Figure 7

RANGE	FLIP-FLOP	
	18a	18b
1	0	0
10	0	1
100	1	0
1000	1	1

Figure 9

NOR GATES	RANGE									
	VAC & KΩ				VDC			MVDC		MΩ
	1	10	100	1000	10	100	1000	100	1000	10
12B	1	0	0	0	0	0	0	0	0	0
10D	0	1	0	0	1	0	0	0	0	0
10B	0	0	1	0	0	1	0	1	0	0
10C	0	0	0	1	0	0	1	0	1	0

Figure 8

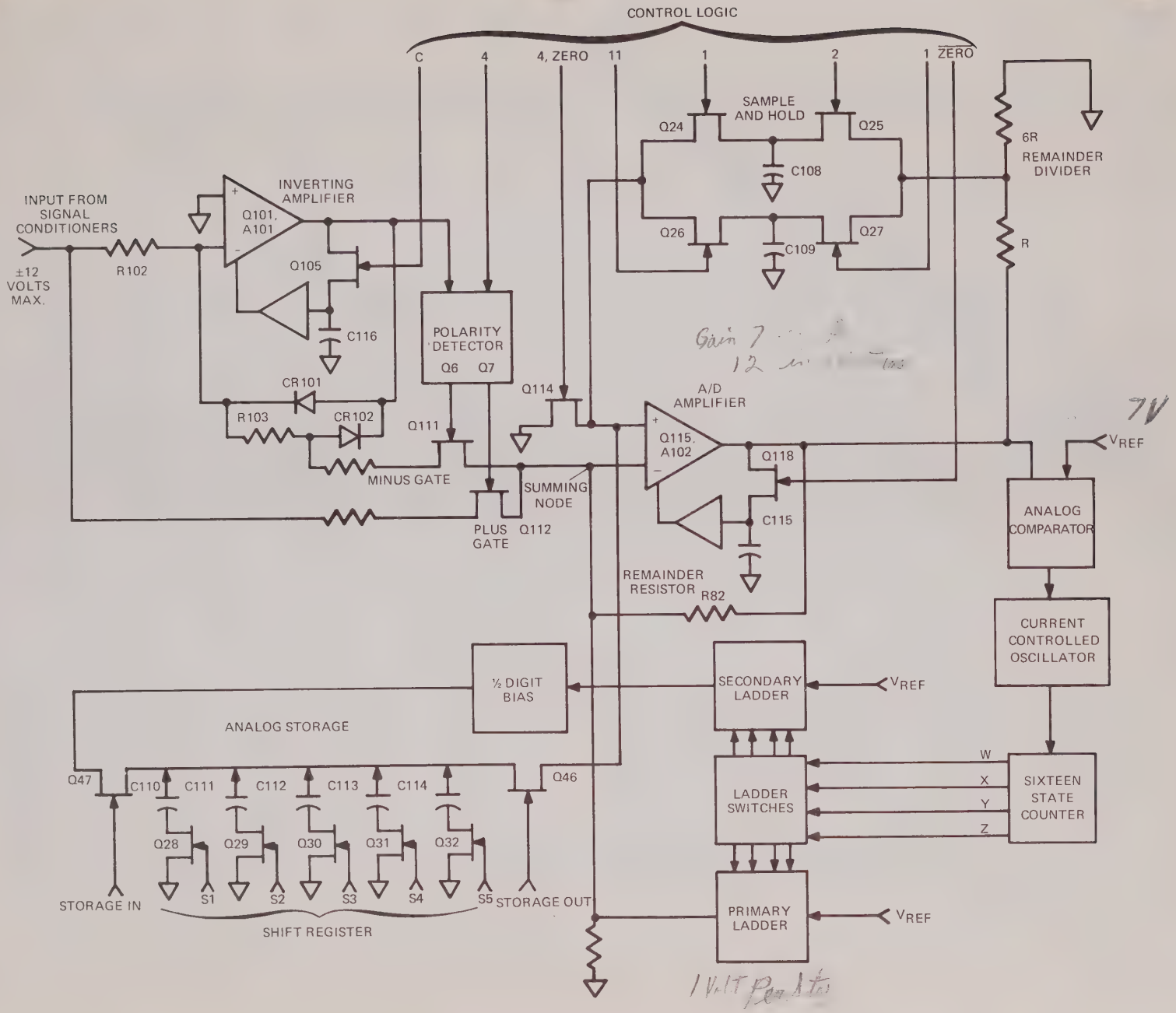


Figure 10. 8300A BLOCK DIAGRAM

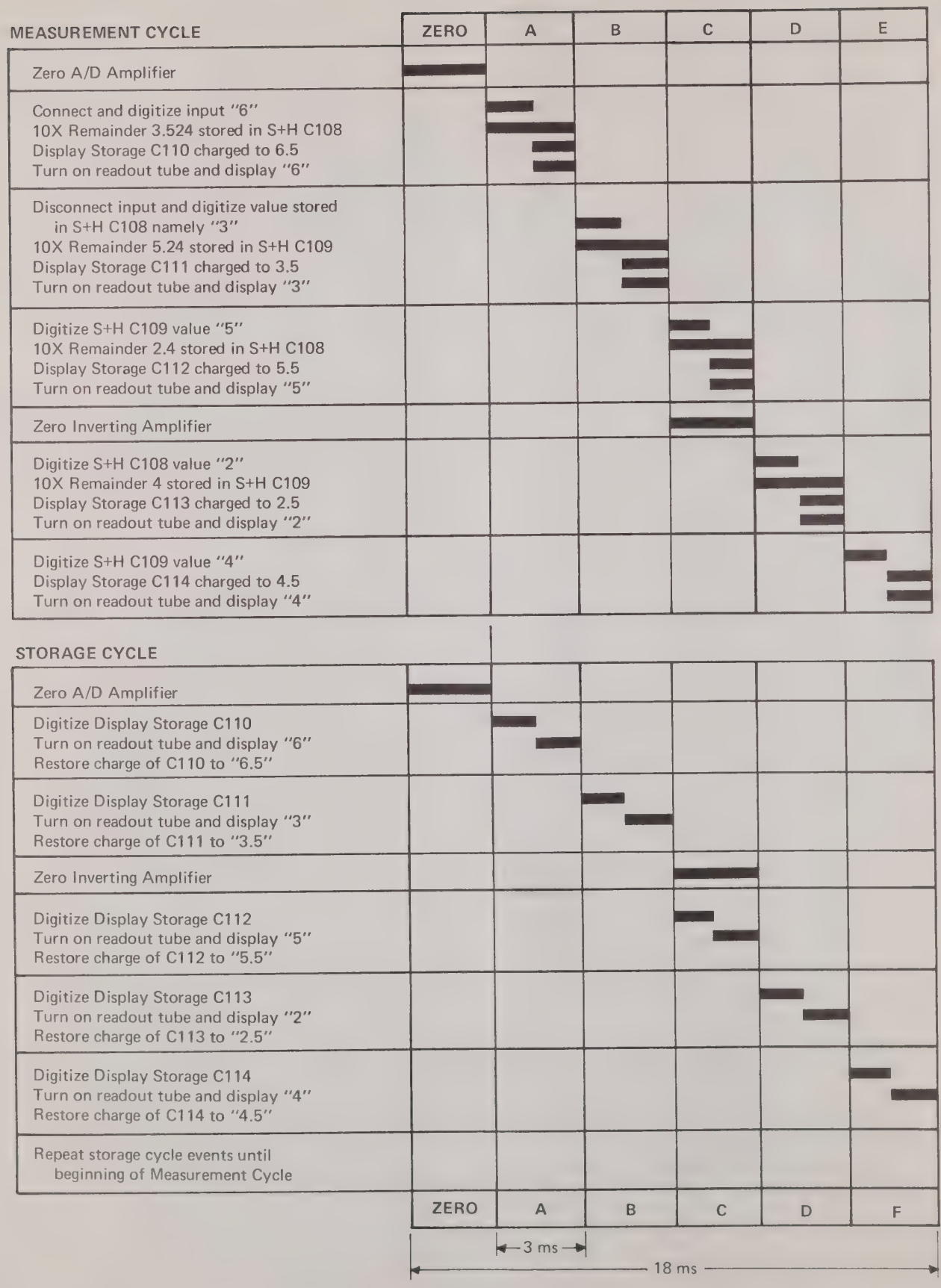
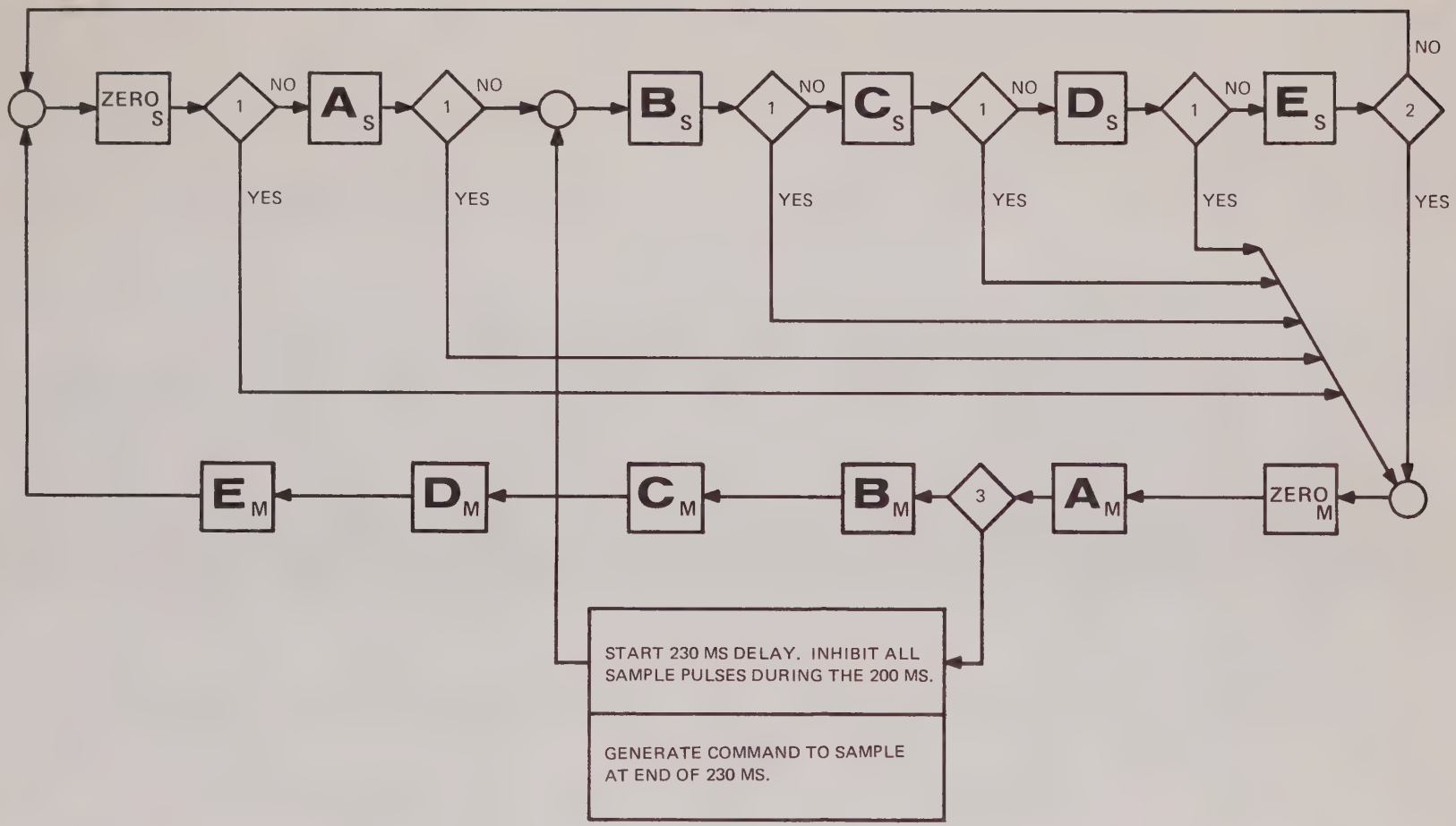

MEASUREMENT CYCLE
ZERO
A
B
C
D
E
Zero A/D Amplifier
Connect and digitize input "6"
10X Remainder 3.524 stored in S+H C108
Display Storage C110 charged to 6.5
Turn on readout tube and display "6"
Disconnect input and digitize value stored in S+H C108 namely "3"
10X Remainder 5.24 stored in S+H C109
Display Storage C111 charged to 3.5
Turn on readout tube and display "3"
Digitize S+H C109 value "5"
10X Remainder 2.4 stored in S+H C108
Display Storage C112 charged to 5.5
Turn on readout tube and display "5"
Zero Inverting Amplifier
Digitize S+H C108 value "2"
10X Remainder 4 stored in S+H C109
Display Storage C113 charged to 2.5
Turn on readout tube and display "2"
Digitize S+H C109 value "4"
Display Storage C114 charged to 4.5
Turn on readout tube and display "4"
STORAGE CYCLE
Zero A/D Amplifier
Digitize Display Storage C110
Turn on readout tube and display "6"
Restore charge of C110 to "6.5"
Digitize Display Storage C111
Turn on readout tube and display "3"
Restore charge of C111 to "3.5"
Zero Inverting Amplifier
Digitize Display Storage C112
Turn on readout tube and display "5"
Restore charge of C112 to "5.5"
Digitize Display Storage C113
Turn on readout tube and display "2"
Restore charge of C113 to "2.5"
Digitize Display Storage C114
Turn on readout tube and display "4"
Restore charge of C114 to "4.5"
Repeat storage cycle events until beginning of Measurement Cycle
ZERO
A
B
C
D
F
3 ms
18 ms

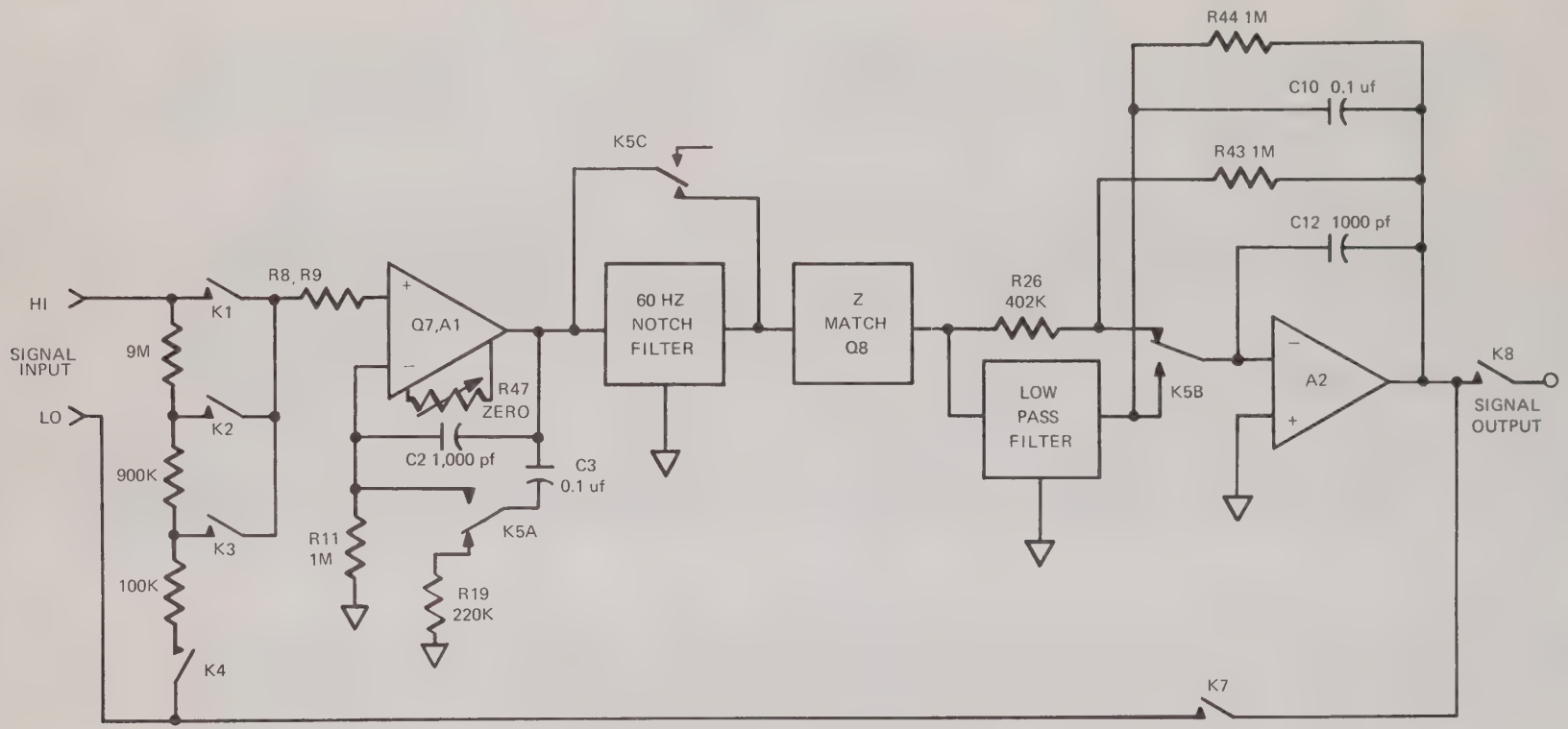
Figure 11.

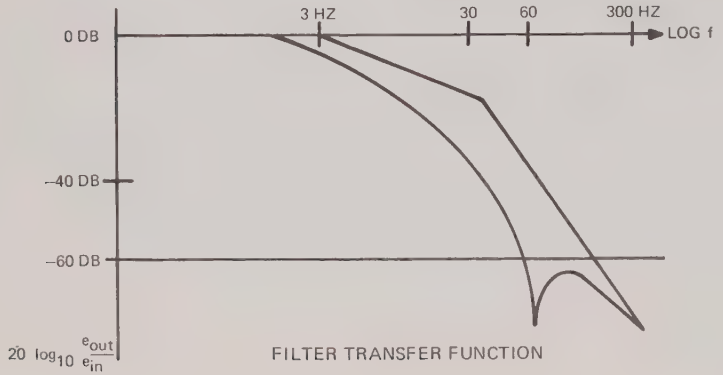


LEGEND:

- ○ RE-ENTRY PATH
- □ 3 MS OPERATION AS INDICATED.
- ◇1 SAMPLE COMMAND RECEIVED DURING PRECEEDING BLOCK AND SAMPLE RATE CONTROL SET TO EXT POSITION.
- ◇2 SAMPLE COMMAND RECEIVED DURING PRECEEDING BLOCK.
- ◇3 REQUIREMENT TO RANGE DETECTED DURING A_M BLOCK.

Figure 12. CYCLE CHANGE FLOW CHART





FILTER TRANSFER FUNCTION

RELAY OPERATION

K1		All KΩ Ranges
		MΩ
		10 VDC
K2	-	100 VDC
K3	-	1000 VDC
		AC
K4		100 VDC
		1000 VDC
K5		Filter and any KΩ, MΩ or DCV
K7		All KΩ, MΩ and DC
K8		All DC, MΩ, 1000 KΩ and 100 KΩ

Figure 13. BUFFER ASSEMBLY BLOCK DIAGRAM

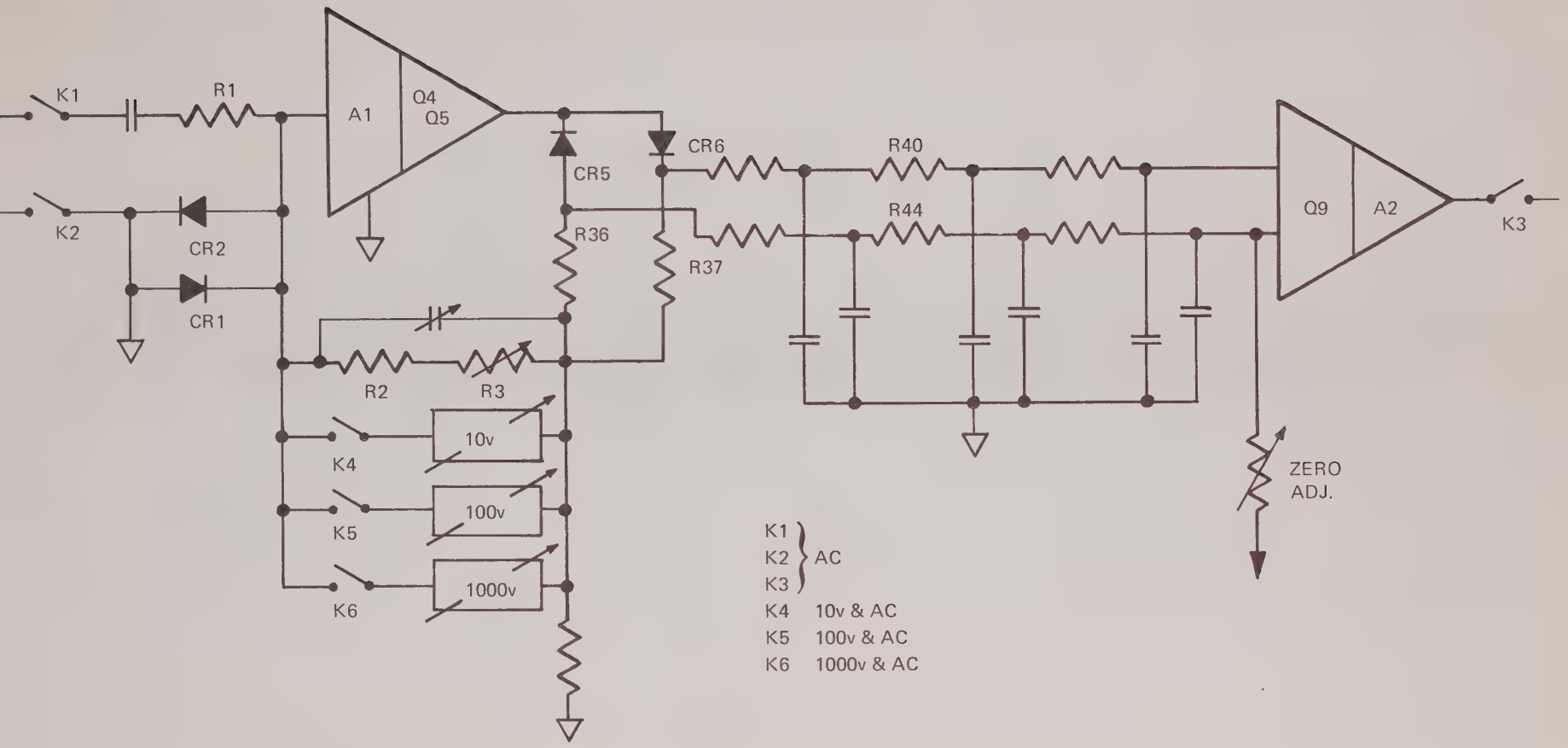
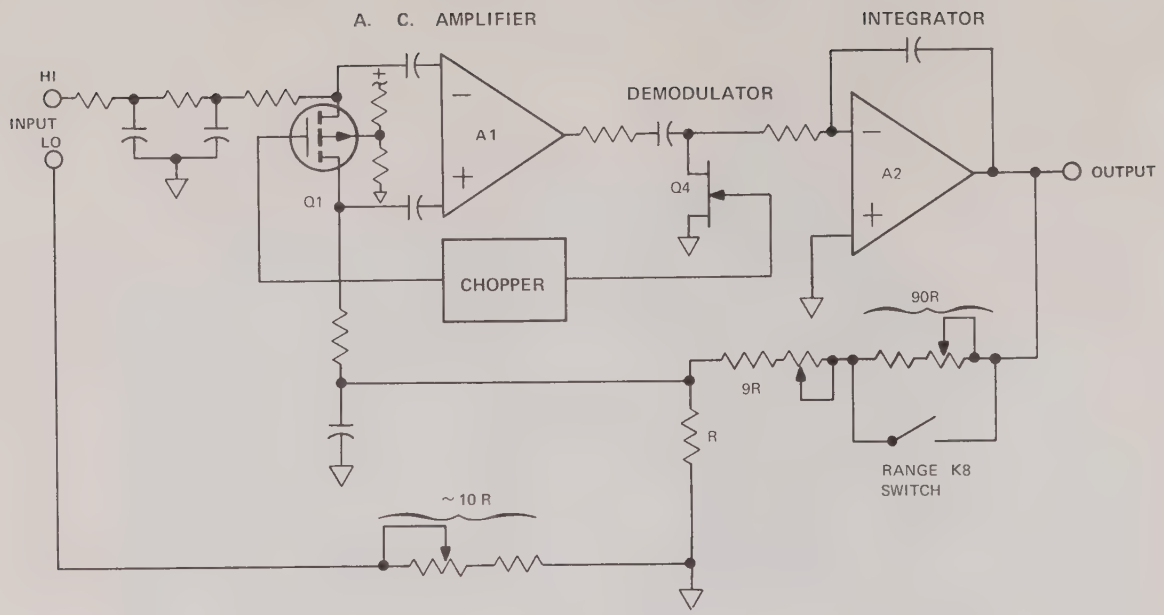
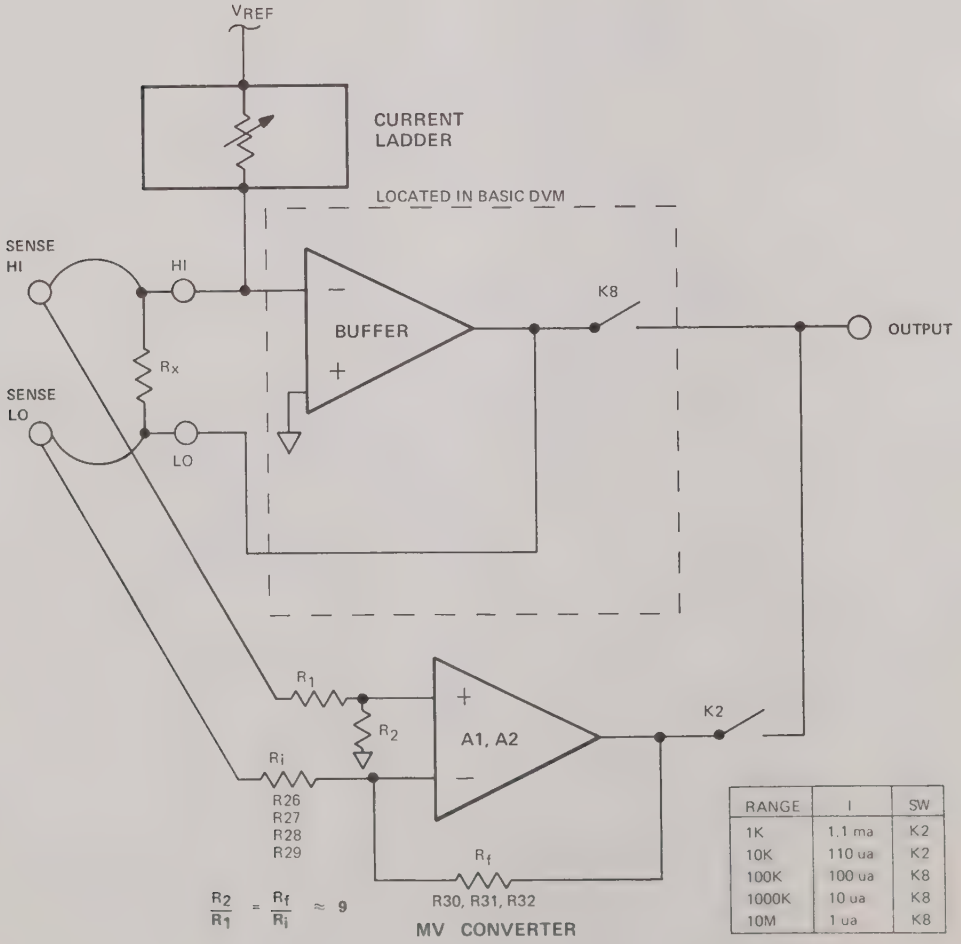


Figure 14. AC CONVERTER OPTION





RANGE	I	SW
1K	1.1 ma	K2
10K	110 ua	K2
100K	100 ua	K8
1000K	10 ua	K8
10M	1 ua	K8

Figure 15.

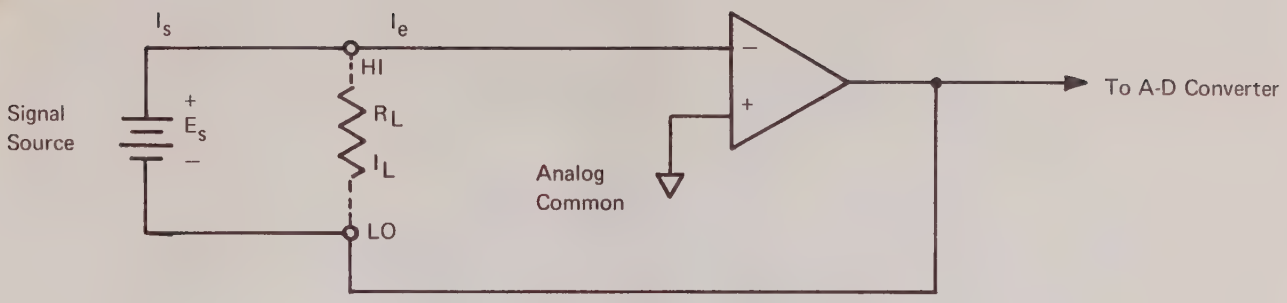


Figure 16. BUFFER

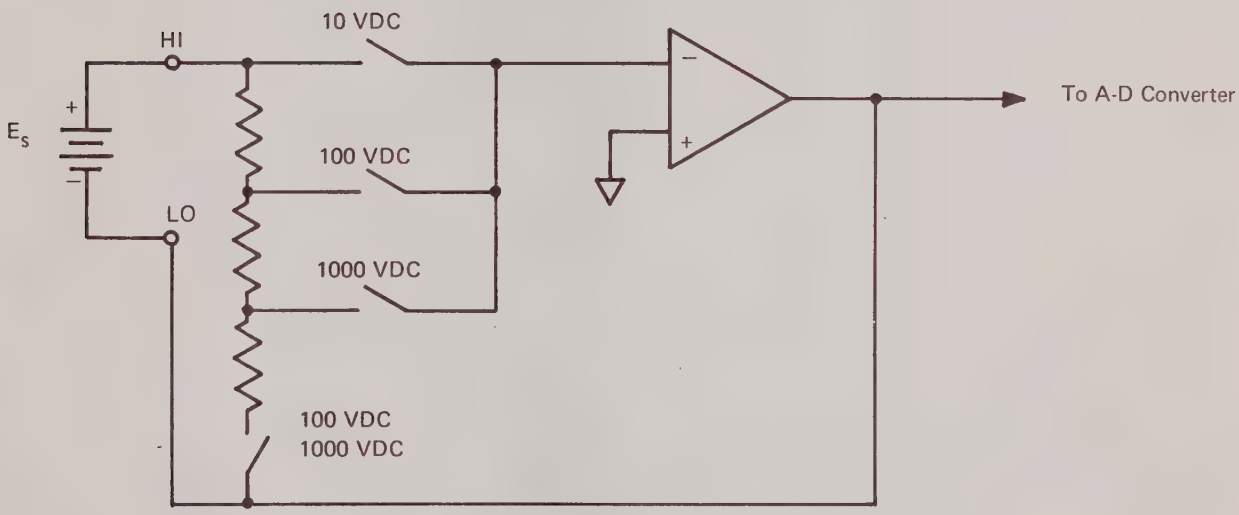


Figure 17. BUFFER WITH ATTENUATOR

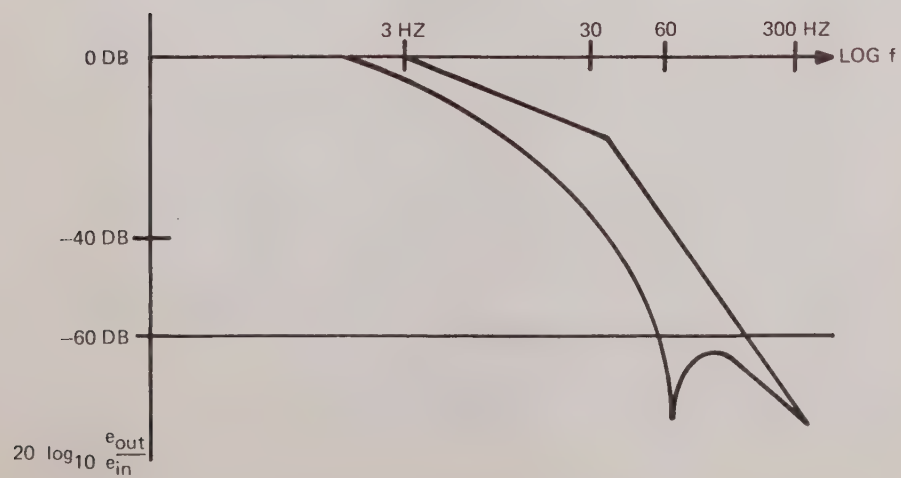
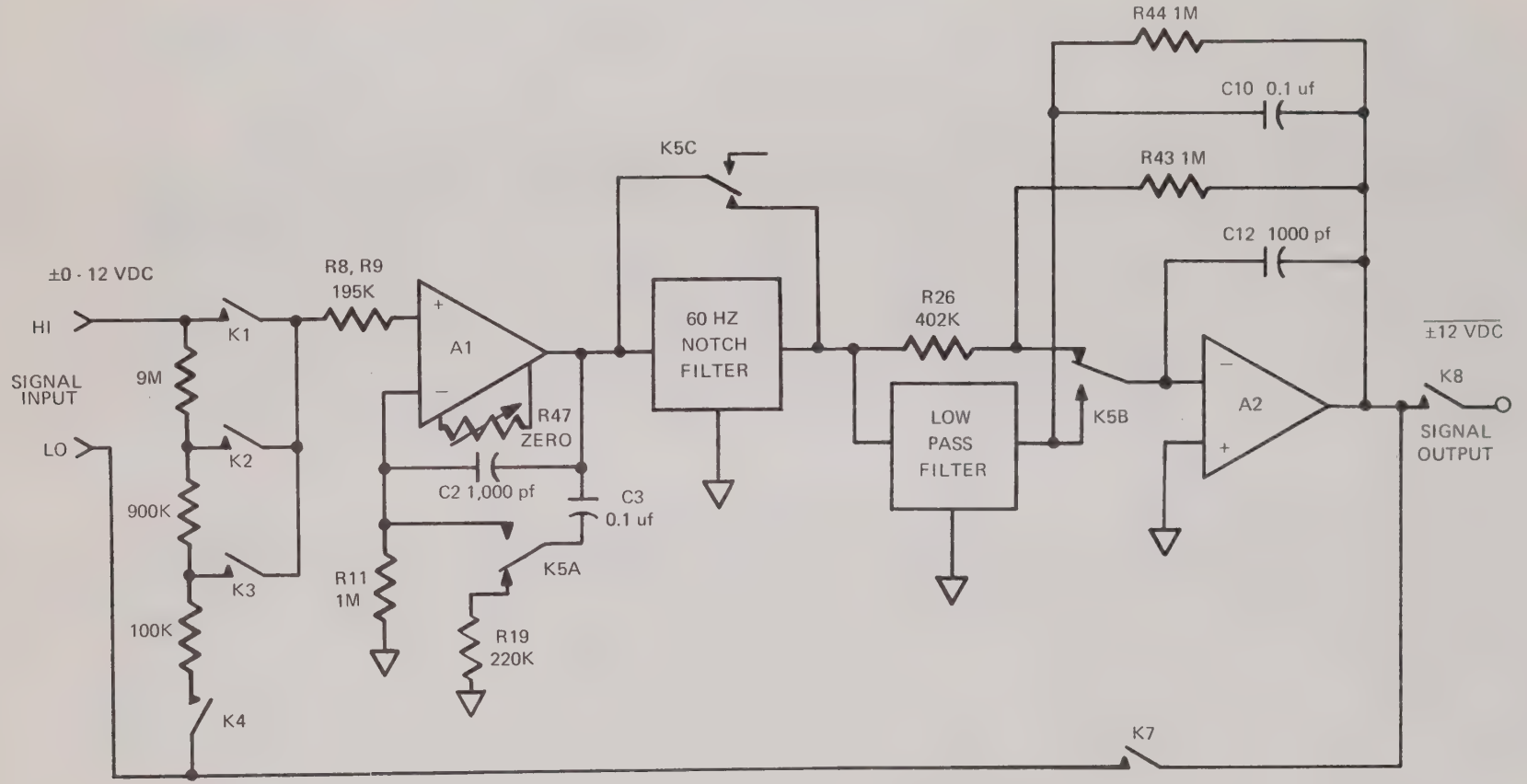


Figure 18. FILTER TRANSFER FUNCTION



RELAY OPERATION

K1	All KΩ Ranges MΩ 10 VDC
K2	100 VDC
K3	1000 VDC
K4	AC 100 VDC 1000 VDC
K5	Filter and any KΩ, MΩ or DCV
K7	All KΩ, MΩ and DC
K8	All DC, MΩ, 1000 KΩ and 100 KΩ

Figure 19. BLOCK DIAGRAM OF BUFFER

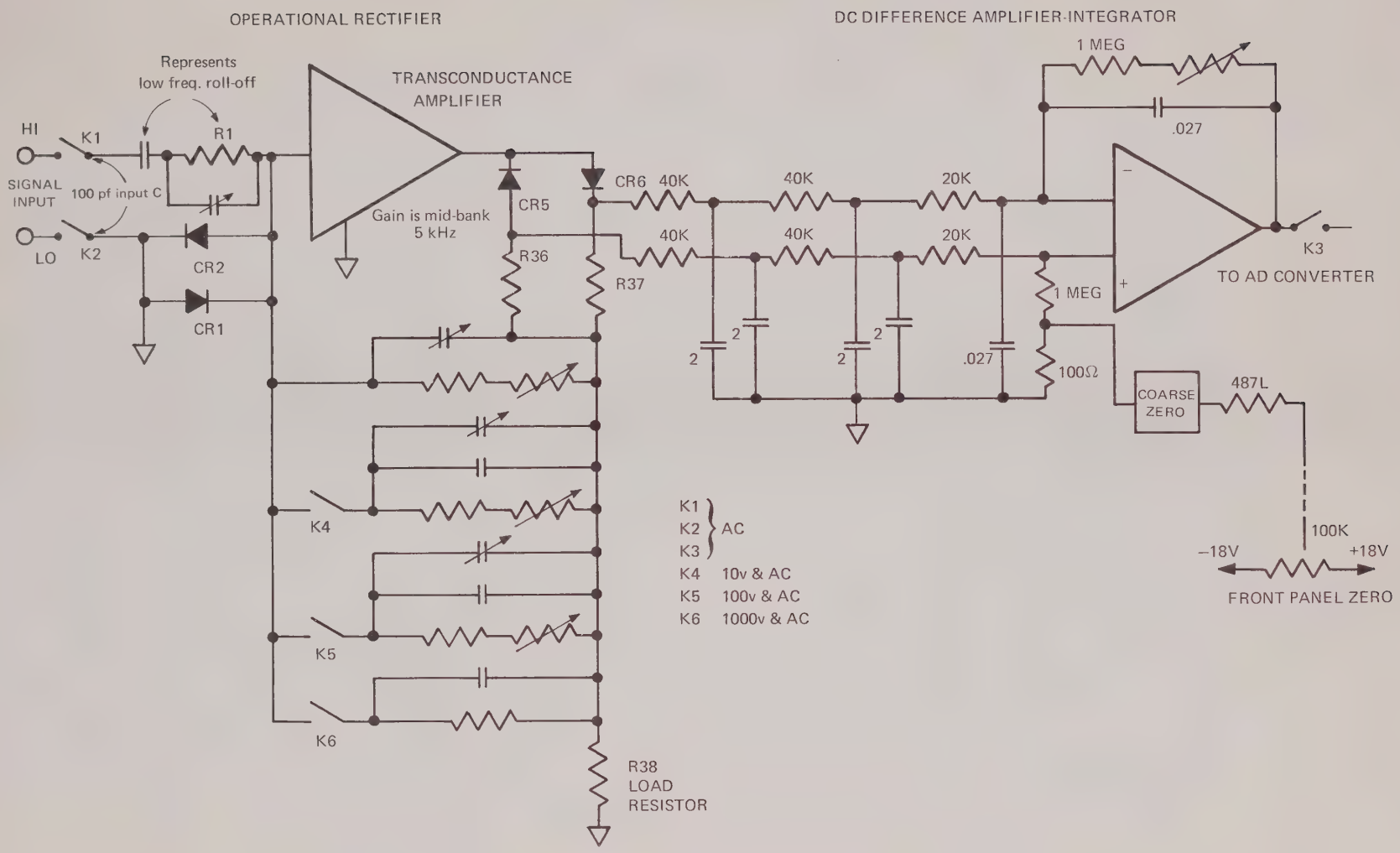


Figure 20. BLOCK DIAGRAM AC CONVERTER

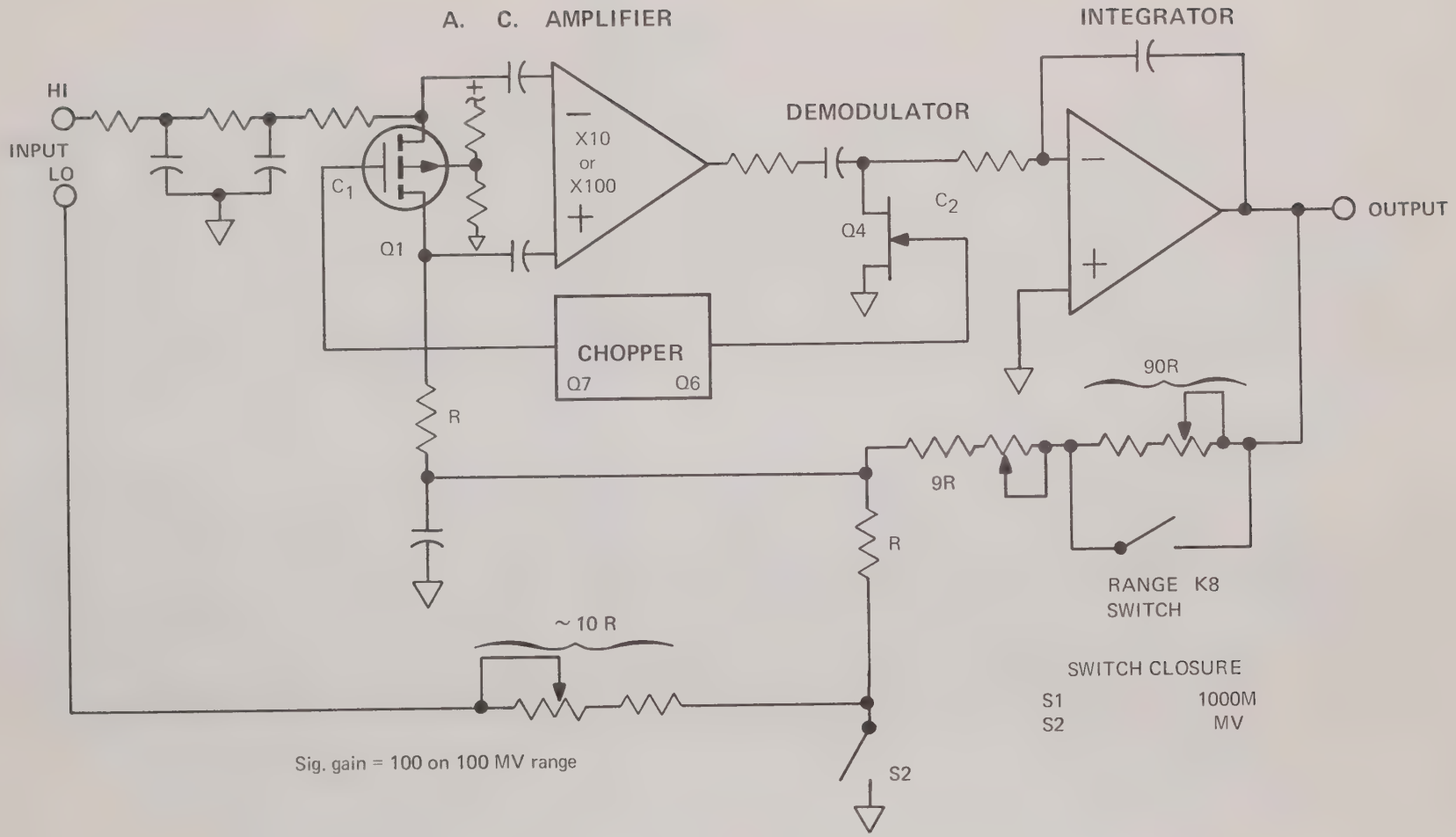
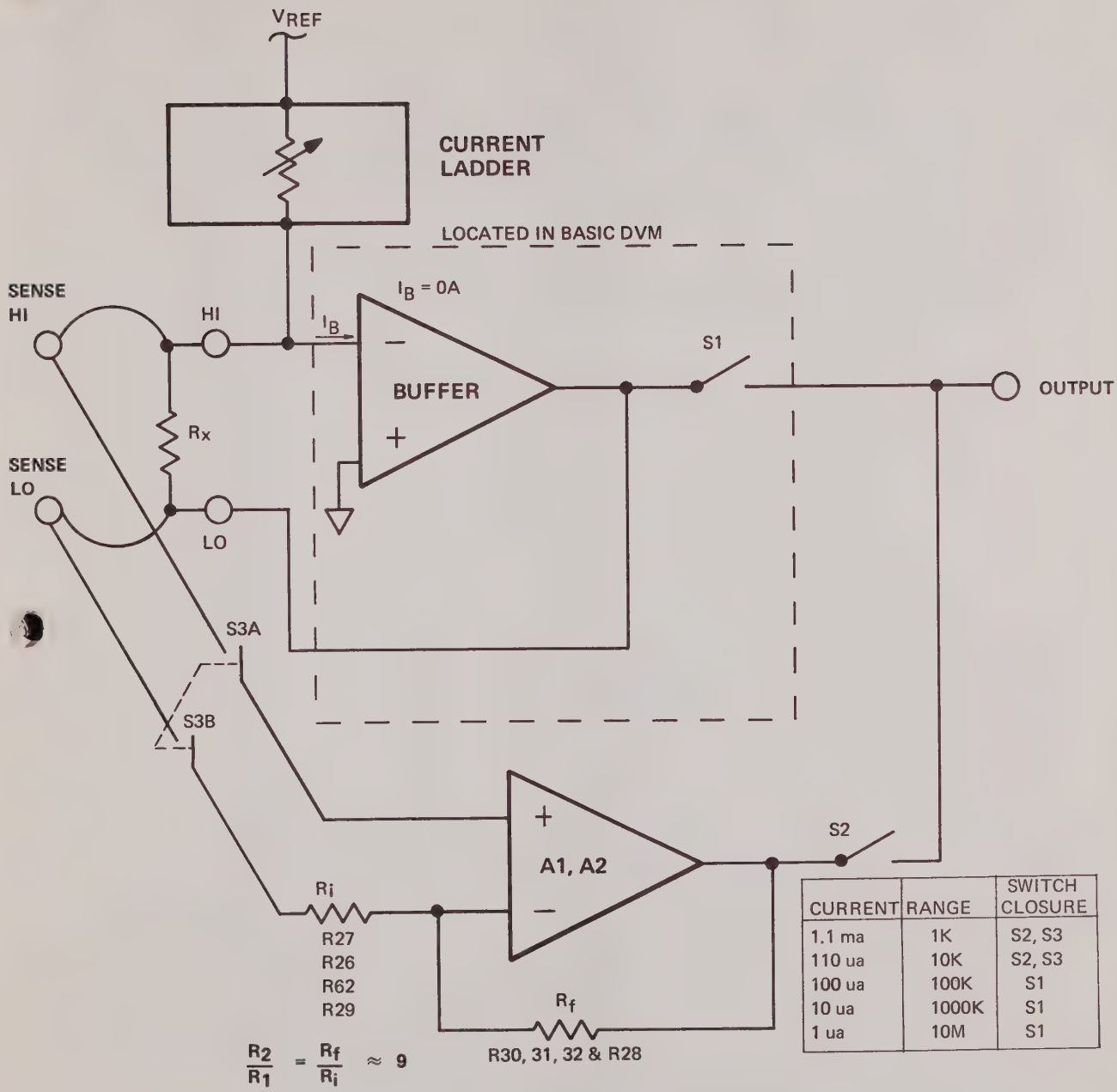


Figure 21. BLOCK DIAGRAM OF MILLIVOLT CONVERTER



CURRENT	RANGE	SWITCH CLOSURE
1.1 ma	1K	S2, S3
110 ua	10K	S2, S3
100 ua	100K	S1
10 ua	1000K	S1
1 ua	10M	S1

Figure 22. BLOCK DIAGRAM OF OHM CONVERTER

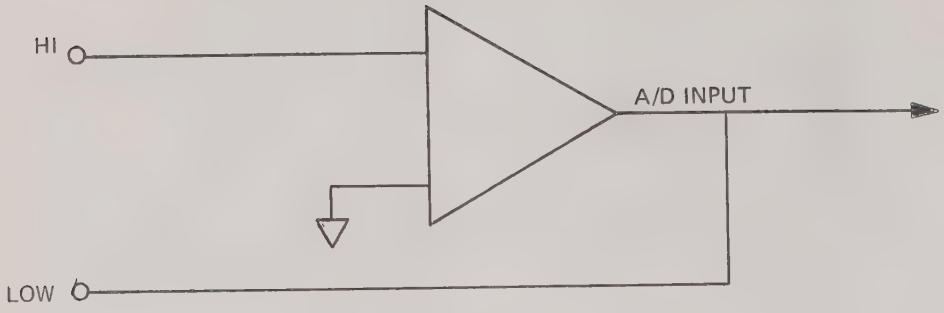


Figure 23.

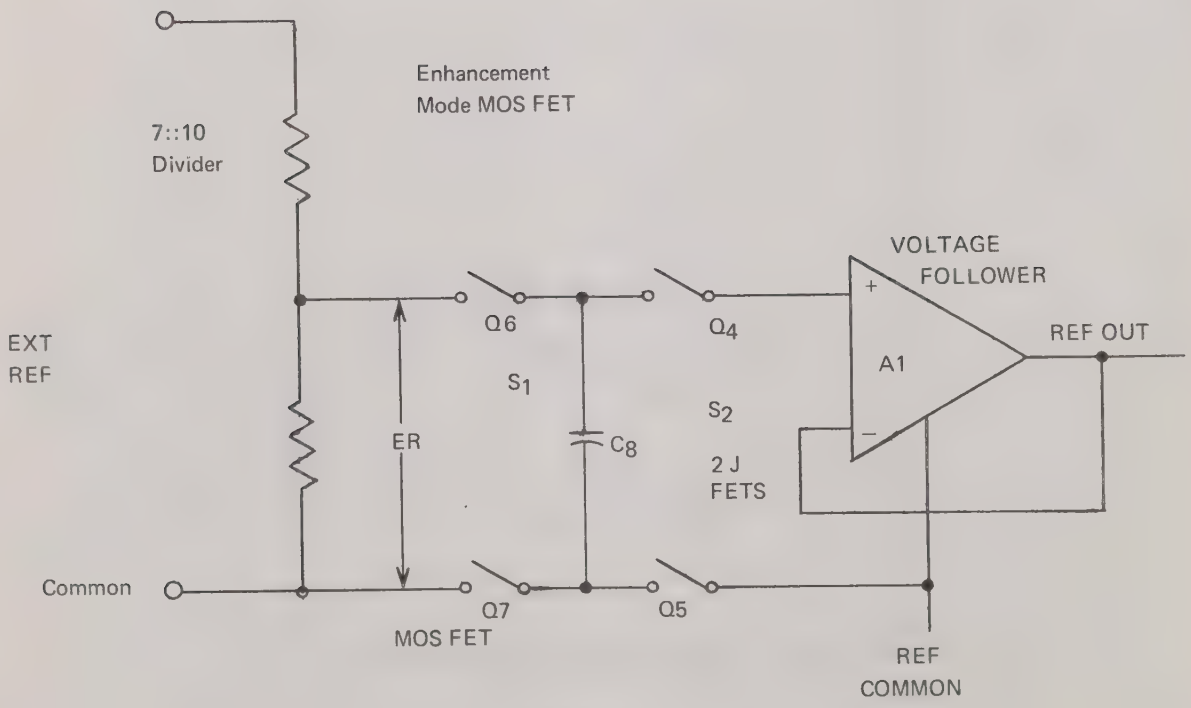


Figure 24.

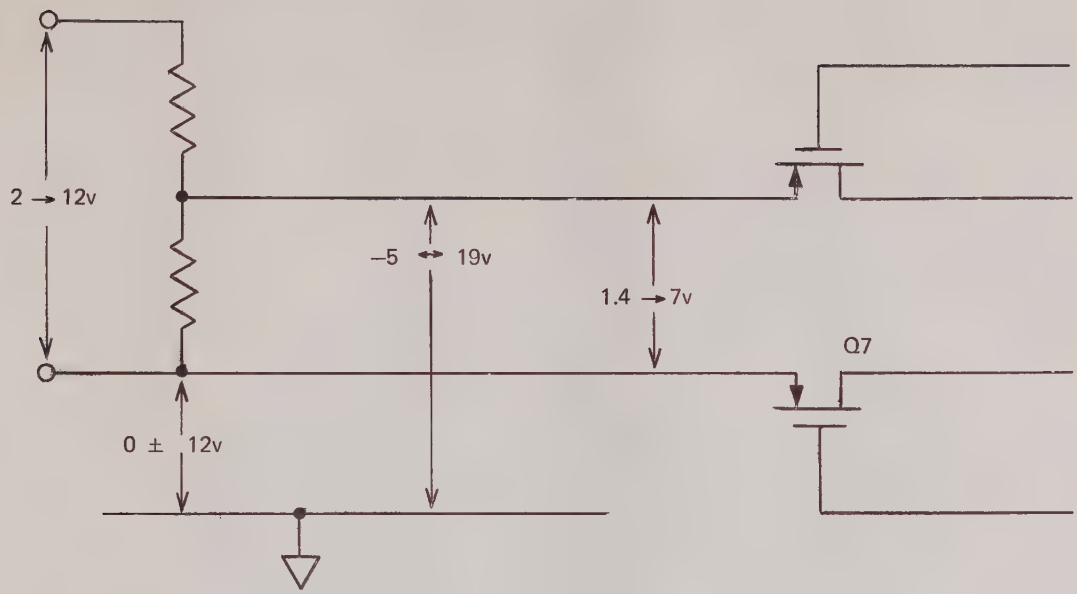


Figure 25

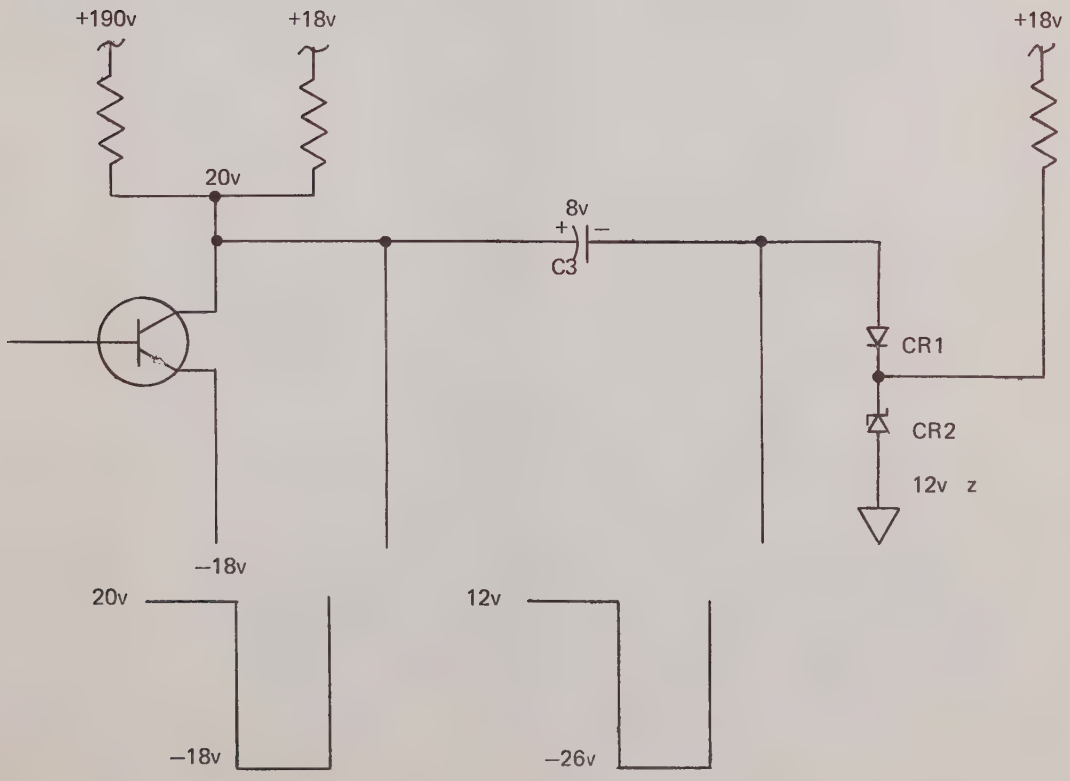


Figure 26

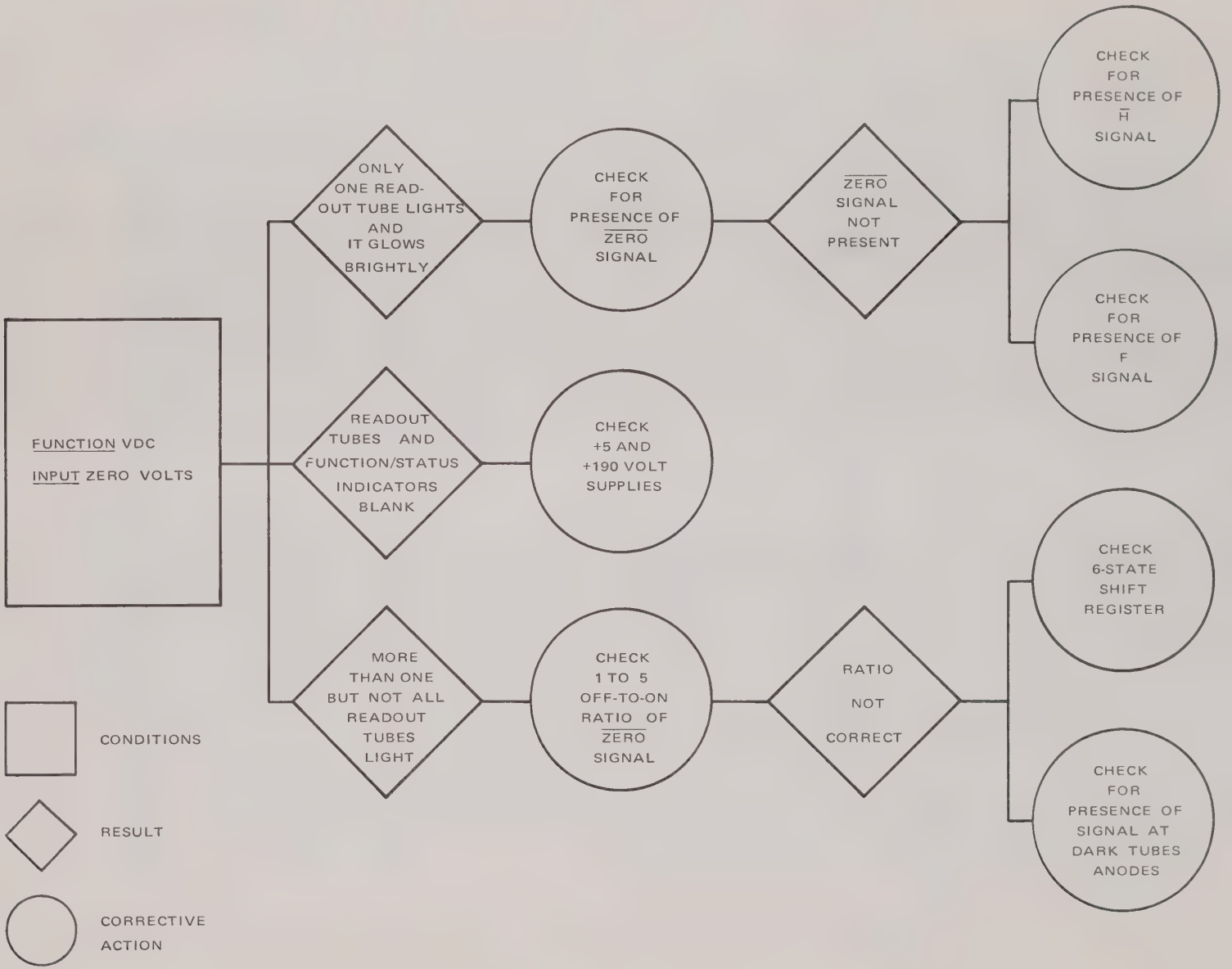

FUNCTION VDC
INPUT ZERO VOLTS
ONLY ONE READ-OUT TUBE LIGHTS AND IT GLOWS BRIGHTLY
READOUT TUBES AND FUNCTION/STATUS INDICATORS BLANK
MORE THAN ONE BUT NOT ALL READOUT TUBES LIGHT
CHECK FOR PRESENCE OF ZERO SIGNAL
CHECK +5 AND +190 VOLT SUPPLIES
CHECK 1 TO 5 OFF-TO-ON RATIO OF ZERO SIGNAL
ZERO SIGNAL NOT PRESENT
RATIO NOT CORRECT
CHECK FOR PRESENCE OF H SIGNAL
CHECK FOR PRESENCE OF F SIGNAL
CHECK 6-STATE SHIFT REGISTER
CHECK FOR PRESENCE OF SIGNAL AT DARK TUBES ANODES
CONDITIONS
RESULT
CORRECTIVE ACTION

Figure 27.

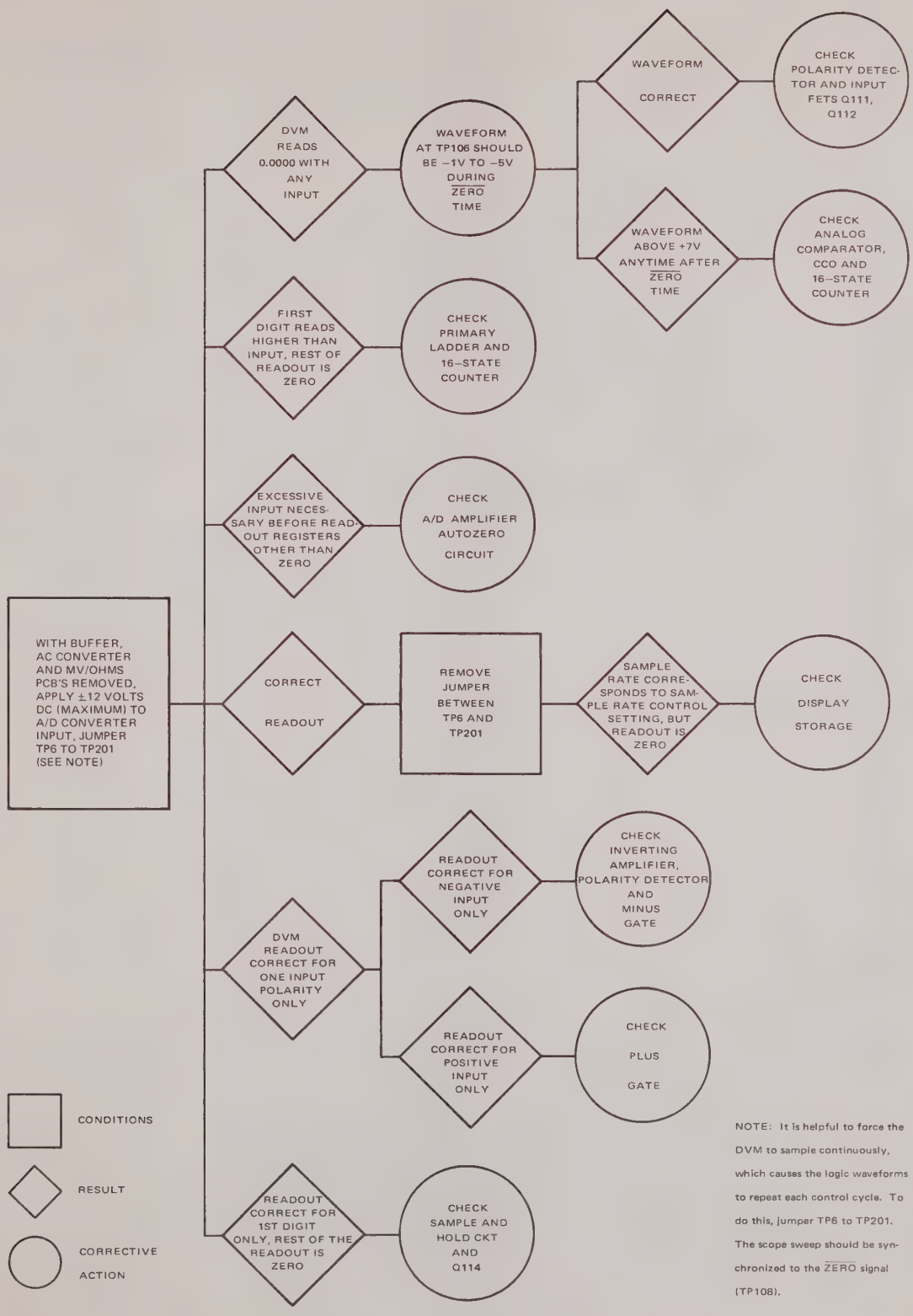
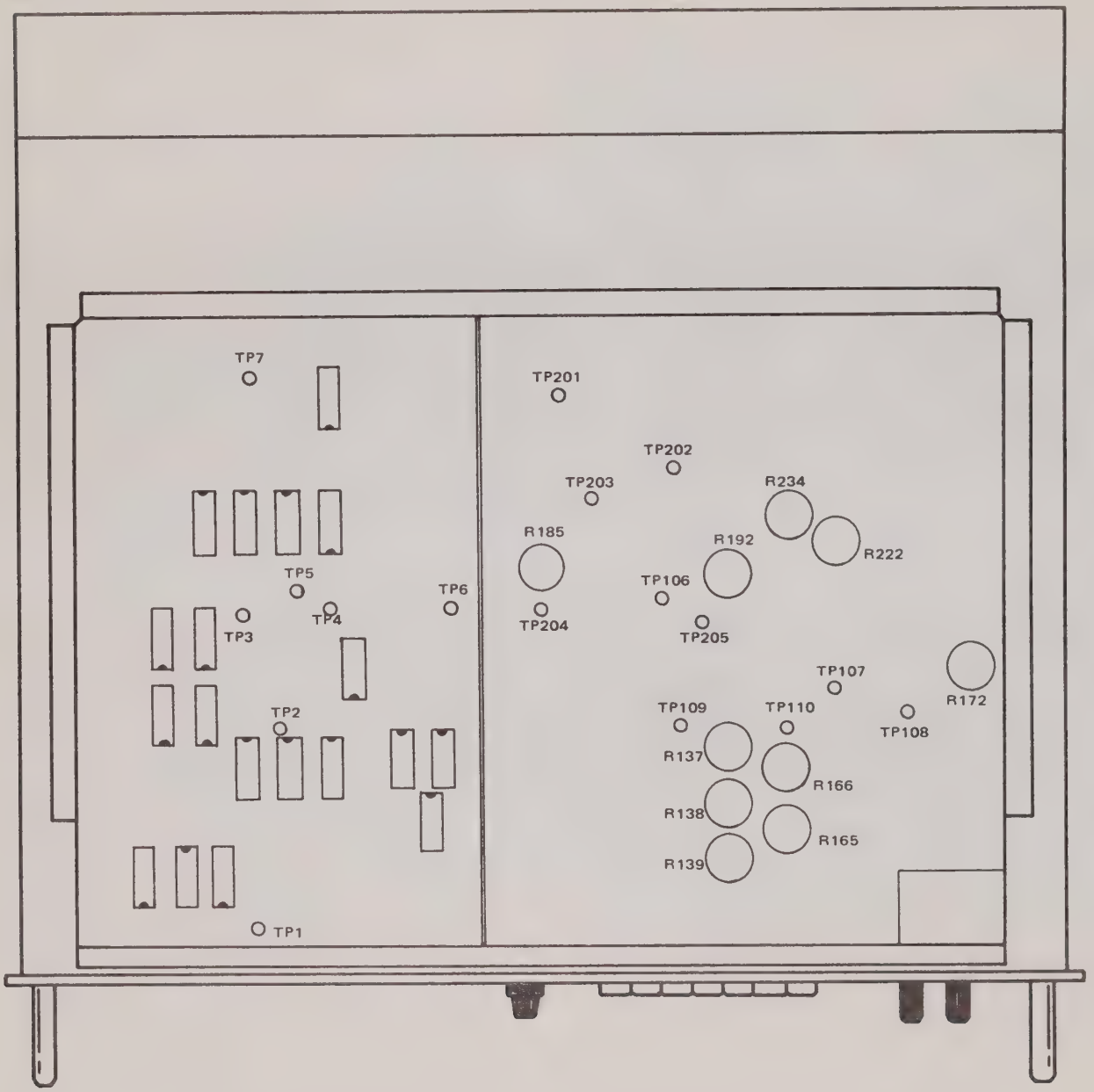

WITH BUFFER, AC CONVERTER AND MV/OHMS PCB'S REMOVED, APPLY ±12 VOLTS DC (MAXIMUM) TO A/D CONVERTER INPUT, JUMPER TP6 TO TP201 (SEE NOTE)
CORRECT READOUT
REMOVE JUMPER BETWEEN TP6 AND TP201
SAMPLE RATE CORRESPONDS TO SAMPLE RATE CONTROL SETTING, BUT READOUT IS ZERO
CHECK DISPLAY STORAGE
DVM READS 0.0000 WITH ANY INPUT
WAVEFORM AT TP106 SHOULD BE −1V TO −5V DURING ZERO TIME
WAVEFORM CORRECT
CHECK POLARITY DETECTOR AND INPUT FETS Q111, Q112
WAVEFORM ABOVE +7V ANYTIME AFTER ZERO TIME
CHECK ANALOG COMPARATOR, CCO AND 16-STATE COUNTER
FIRST DIGIT READS HIGHER THAN INPUT, REST OF READOUT IS ZERO
CHECK PRIMARY LADDER AND 16-STATE COUNTER
EXCESSIVE INPUT NECESSARY BEFORE READOUT REGISTERS OTHER THAN ZERO
CHECK A/D AMPLIFIER AUTOZERO CIRCUIT
DVM READOUT CORRECT FOR ONE INPUT POLARITY ONLY
READOUT CORRECT FOR NEGATIVE INPUT ONLY
CHECK INVERTING AMPLIFIER, POLARITY DETECTOR AND MINUS GATE
READOUT CORRECT FOR POSITIVE INPUT ONLY
CHECK PLUS GATE
READOUT CORRECT FOR 1ST DIGIT ONLY, REST OF THE READOUT IS ZERO
CHECK SAMPLE AND HOLD CKT AND Q114
CONDITIONS
RESULT
CORRECTIVE ACTION
NOTE: It is helpful to force the DVM to sample continuously, which causes the logic waveforms to repeat each control cycle. To do this, jumper TP6 to TP201. The scope sweep should be synchronized to the ZERO signal (TP108).

Figure 28. TROUBLESHOOTING DVM ANALOG CIRCUITRY



TP 1	+190 Anode Strobe
TP 2	H (Clock)
TP 3	Ground
TP 4	$\overline{\text{ZERO}}$
TP 5	F
TP 6	Trigger Input
TP 7	Range Pulsing
TP 106	A/D Amp. Out
TP 107	VCO
TP 108	$\overline{\text{ZERO}}$
TP 109	Ground
TP 110	Pri. Ladder Out
TP 111	Inv. Amp. Out
TP 201	+5v
TP 202	+190v
TP 203	−18v
TP 204	+18v
TP 205	+7v
R 137	Ladder Cal 4
R 138	Ladder Cal 2
R 139	Ladder Cal 1
R 165	− Cal
R 166	+ Cal
R 172	Comparator Level
R 185	Remainder Cal
R 192	A-D Zero
R 222	+7v Ref.
R 234	+18v

Figure 29.

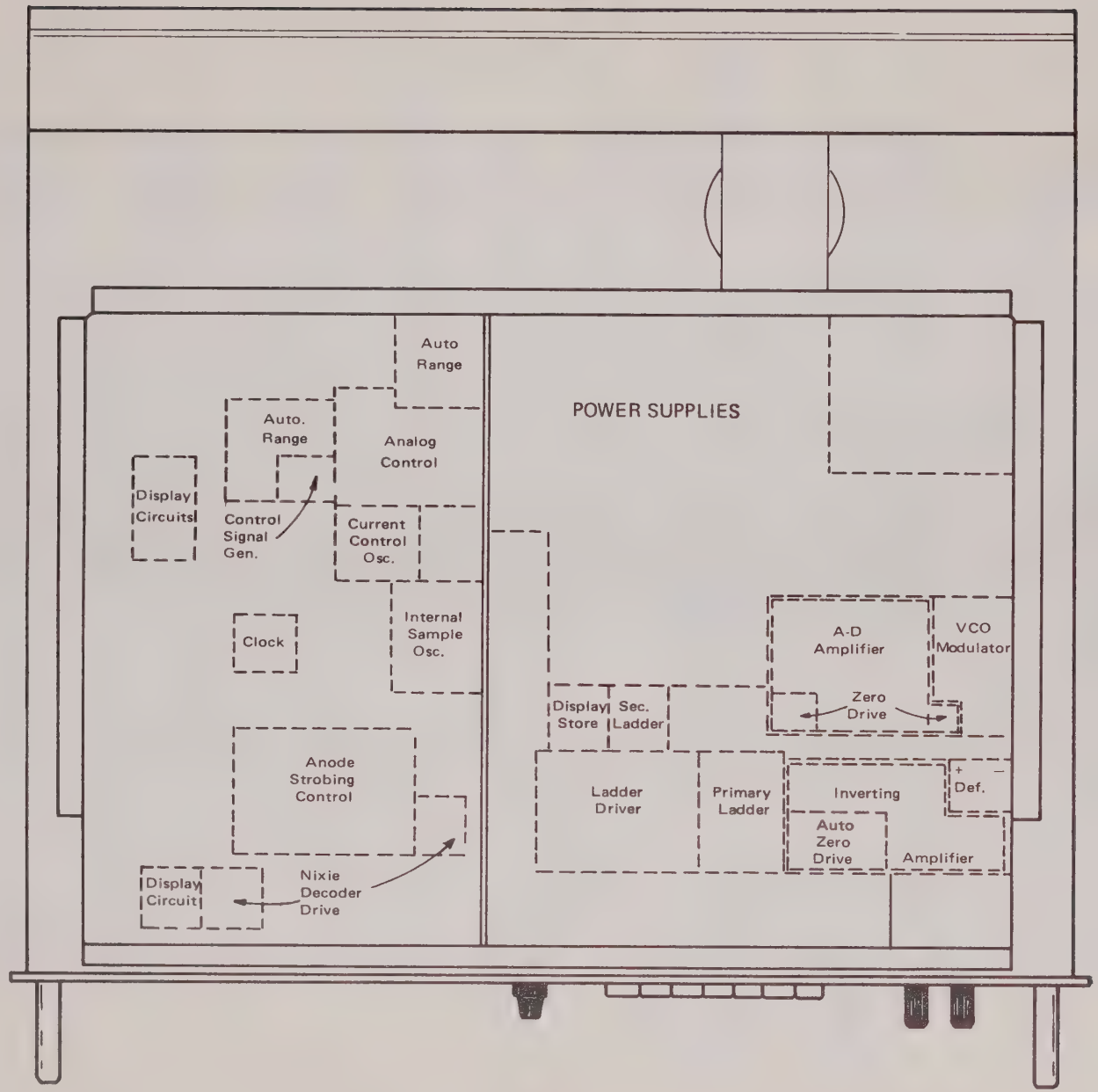
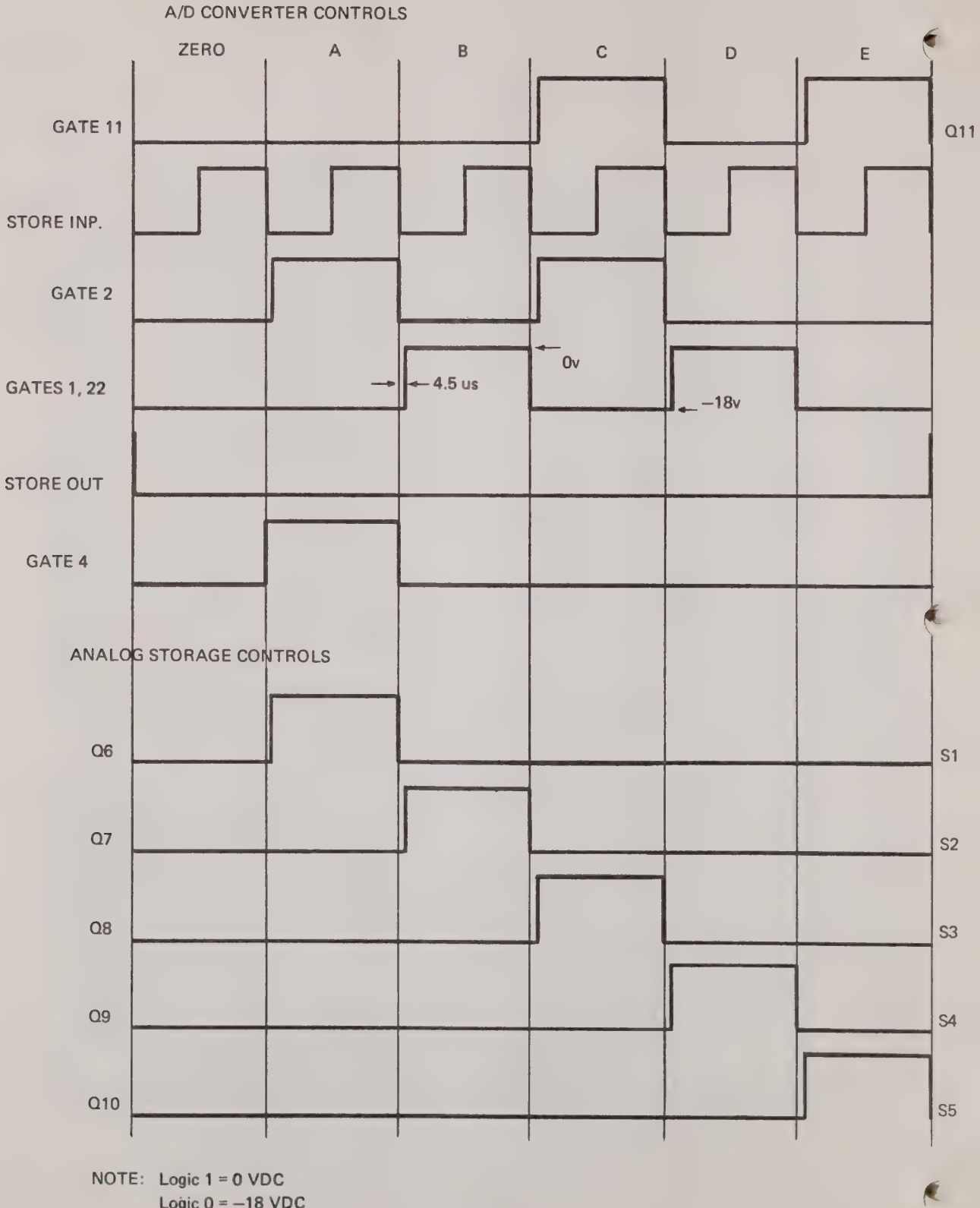

Auto
Range
POWER SUPPLIES
Auto.
Range
Analog
Control
Display
Circuits
Control
Signal
Gen.
Current
Control
Osc.
Internal
Sample
Osc.
Clock
A-D
Amplifier
VCO
Modulator
Zero
Drive
Display
Store
Sec.
Ladder
Anode
Strobing
Control
Ladder
Driver
Primary
Ladder
Inverting
Def.
Auto
Zero
Drive
Amplifier
Display
Circuit
Nixie
Decoder
Drive

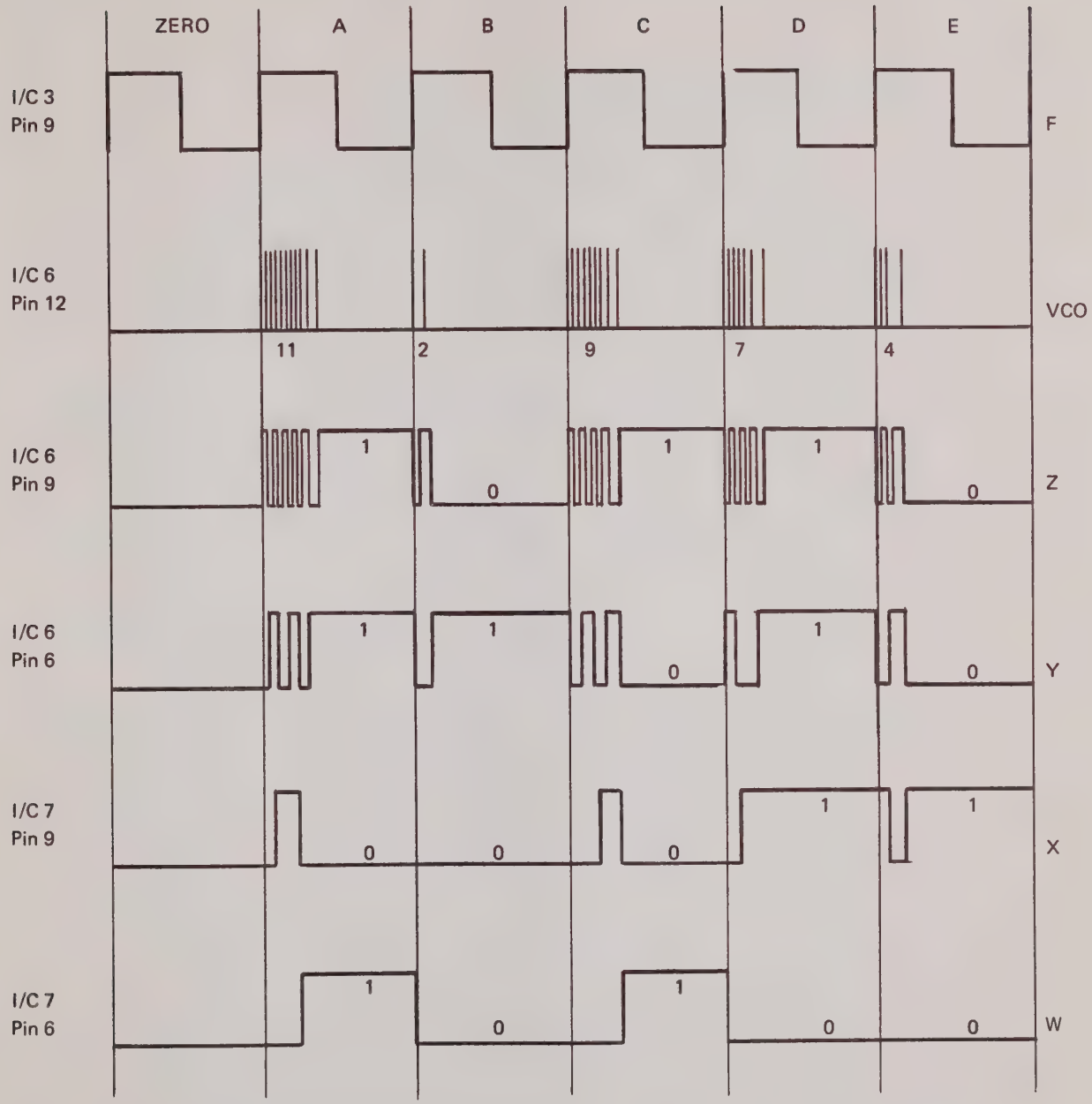
Figure 30.



NOTE: Logic 1 = 0 VDC
Logic 0 = −18 VDC

Figure 31.

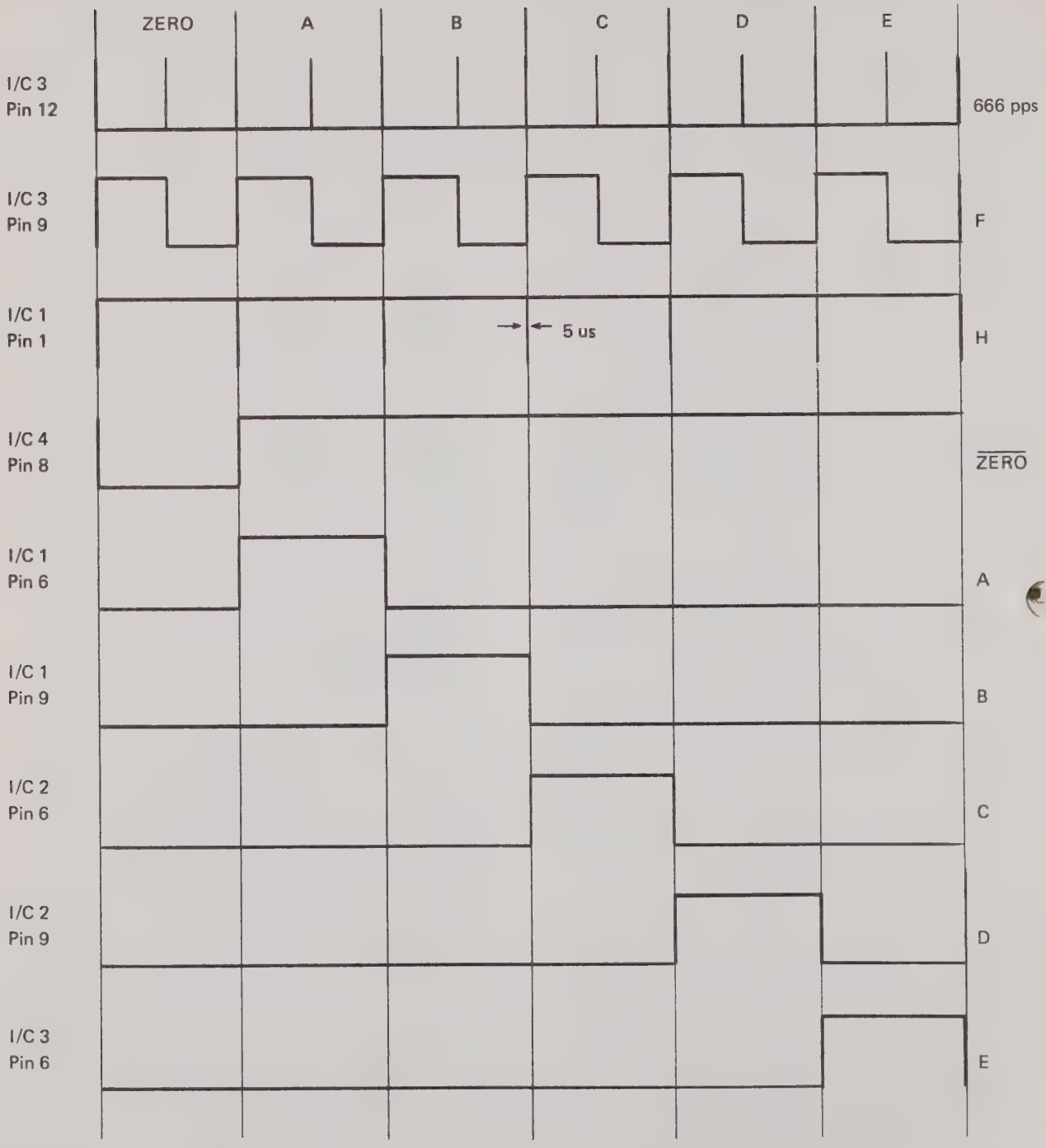
16 STATE BINARY COUNTER OPERATION



NOTE: Example display is 11.2974v
Logic 0 = < 0.5v
Logic 1 = > 3.5v

Figure 32.

SHIFT REGISTER OPERATION



NOTE: Logic 0 = < 0.5v
Logic 1 = > 3.5v

Figure 33.

LOGIC FUNCTIONS (Basic Instrument)

IC 12 Pin 14	$1\ \overline{VDC}\ \overline{M\Omega}\ \overline{MV}$
IC 10 Pin 14	$10\ \overline{MV}$
IC 10 Pin 3	$100\ \overline{M\Omega}$
IC 10 Pin 13	$1000\ \overline{M\Omega}$
IC 11 Pin 2	$\overline{1\ \overline{VDC}\ \overline{Mv} + M\Omega + 10\ \overline{MV}}$
IC 11 Pin 14	$\overline{100\ \overline{M\Omega} + MV + 1000\ \overline{M\Omega}}$
IC 12 Pin 2	$\overline{10\ \overline{MV} + M\Omega + 1000 + DC\bar{a}\bar{b}}$
IC 10 Pin 2	$\overline{100\ \overline{M\Omega} + 1\ \overline{VDC}\ \overline{M\Omega}\ \overline{MV}}$
IC 4 Pin 6	$\bar{a}\bar{b} + \bar{a}VDC + \bar{b}MV + 100 + 10\ \overline{MV} + M\Omega + \overline{\overline{W}\overline{X}\overline{Y}\overline{Z}} + 1000$
IC15 Pin 11	$\overline{\bar{a}\bar{b} + \bar{a}VDC + \bar{b}MV}$
IC 15 Pin 6	$\bar{a} + MV$
IC 15 Pin 3	$\bar{b} + VDC$
IC 15 Pin 8	$\overline{WX}$
IC 13 Pin 13	WXb
IC 13 Pin 14	$a\bar{b}\ \bar{a}\overline{VDC}\ \bar{b}\overline{MV}\ \overline{100}\ \overline{1000}\ \overline{10\ \overline{MV}}\ \overline{M\Omega}\ \overline{W}\overline{X}\overline{Y}\overline{Z}$
IC 19 Pin 6	$(UP + DN)\ A$
IC 19 Pin 8	$\overline{UP}\ \overline{DN} + \overline{A} + F + \overline{M}$
IC 8 Pin 2	$WYZ\ (1\ \overline{VDC}\ \overline{MV} + 10\ \overline{MV} + 100 + M\Omega + ab)$
IC 8 Pin 14	$\overline{1\ \overline{VDC}\ \overline{MV} + 10\ \overline{MV} + 100 + M\Omega + ab}$
IC 9 Pin 13	$WZ\overline{A}$
IC 9 Pin 14	$\bar{F}EM$
IC 16 Pin 3	ab
IC 11 Pin 13	$VDC\ \bar{a}\bar{b}$
IC 17 Pin 16	$\overline{\overline{W}\overline{X}\overline{Y}\overline{Z} + W\overline{X}YZ}$
IC 17 Pin 15	$\overline{\overline{W}\overline{X}\overline{Y}Z + W\overline{X}YZ}$
IC 17 Pin 8	$\overline{\overline{W}\overline{X}Y\overline{Z} + WX\overline{Y}\overline{Z}}$
IC 17 Pin 9	$\overline{\overline{W}\overline{X}YZ + WX\overline{Y}Z}$
IC 17 Pin 13	$\overline{\overline{W}X\overline{Y}\overline{Z} + WXY\overline{Z}}$
IC 17 Pin 14	$\overline{\overline{W}X\overline{Y}Z + WXYZ}$
IC 17 Pin 11	$\overline{\overline{W}XY\overline{Z}}$
IC 17 Pin 12	$\overline{\overline{W}XYZ}$
IC 17 Pin 1	$\overline{W\overline{X}\overline{Y}\overline{Z}}$
IC 17 Pin 2	$\overline{W\overline{X}\overline{Y}Z}$
Q11 Collector	$M\overline{H}$ (C+E)
Q12 Collector	F
Q13 Collector	$M\overline{H}$ (A+C)
Q14 Collector	$M\overline{H}$ (B+D)
Q15 Collector	$\overline{M}$
Q16 Collector	MA
Q36 Collector	$\bar{F}E$
Q37 Collector	$\bar{F}D$
Q38 Collector	$\bar{F}C$

Figure 34. LOGIC FUNCTIONS (Sheet 1 of 2)

LOGIC FUNCTIONS (Continued)

Q39 Collector	$\bar{F}B$
Q40 Collector	$\bar{F}A$
Q41 Collector	$\overline{WY}$
Q21 Collector	$\bar{a}\bar{b}$
Q22 Collector	$\bar{a}b$
Q23 Collector	$a\bar{b}$
Q24 Collector	ab
Q6 Collector	$A\bar{H}$
Q7 Collector	$B\bar{H}$
Q8 Collector	$C\bar{H}$
Q9 Collector	$D\bar{H}$
Q10 Collector	$E\bar{H}$
Q29 Emitter	a buffered
Q30 Emitter	b buffered

Figure 34. LOGIC FUNCTIONS (Sheet 2 of 2)

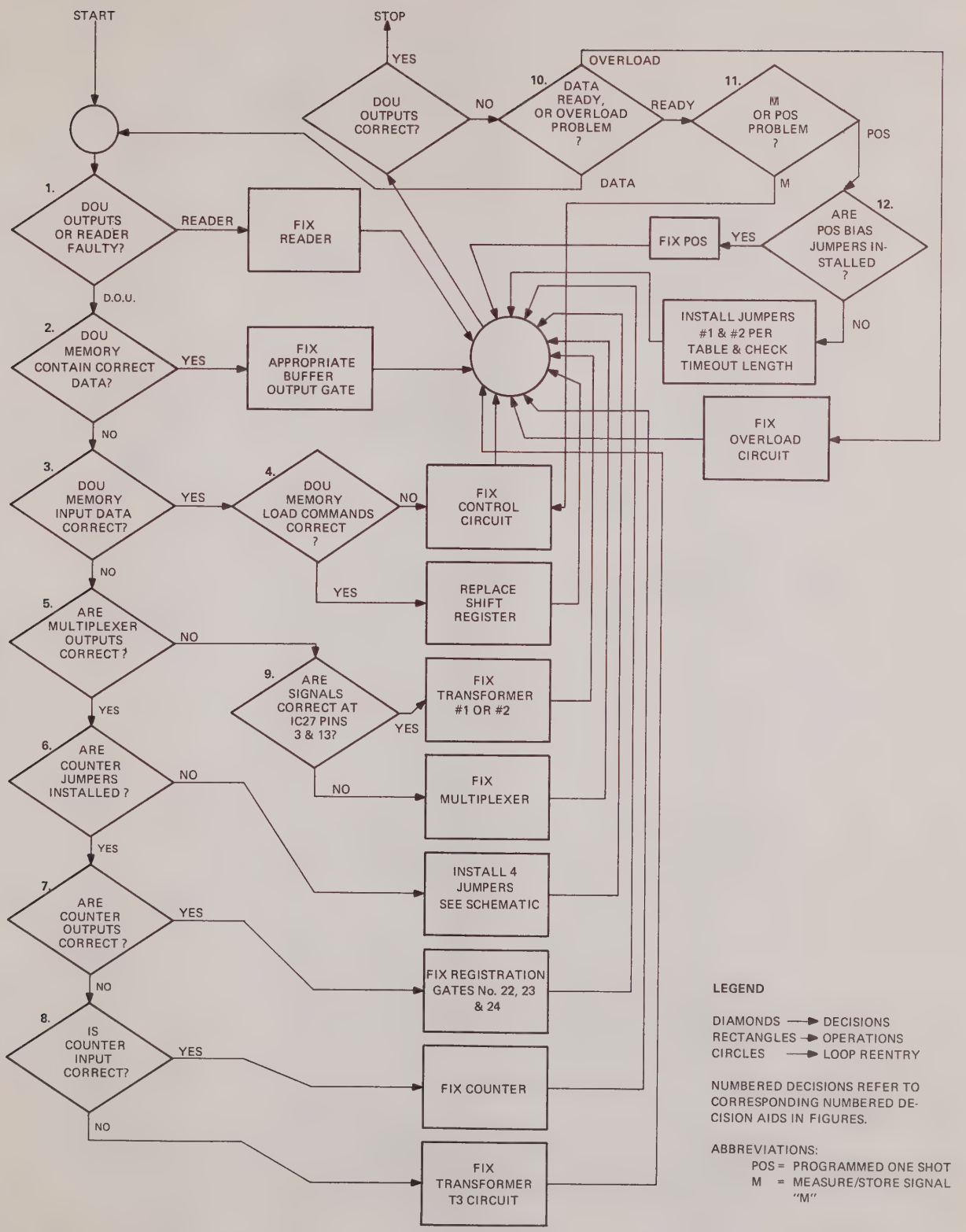


Figure 35. DECISION FLOW CHART —DOU TROUBLESHOOTING

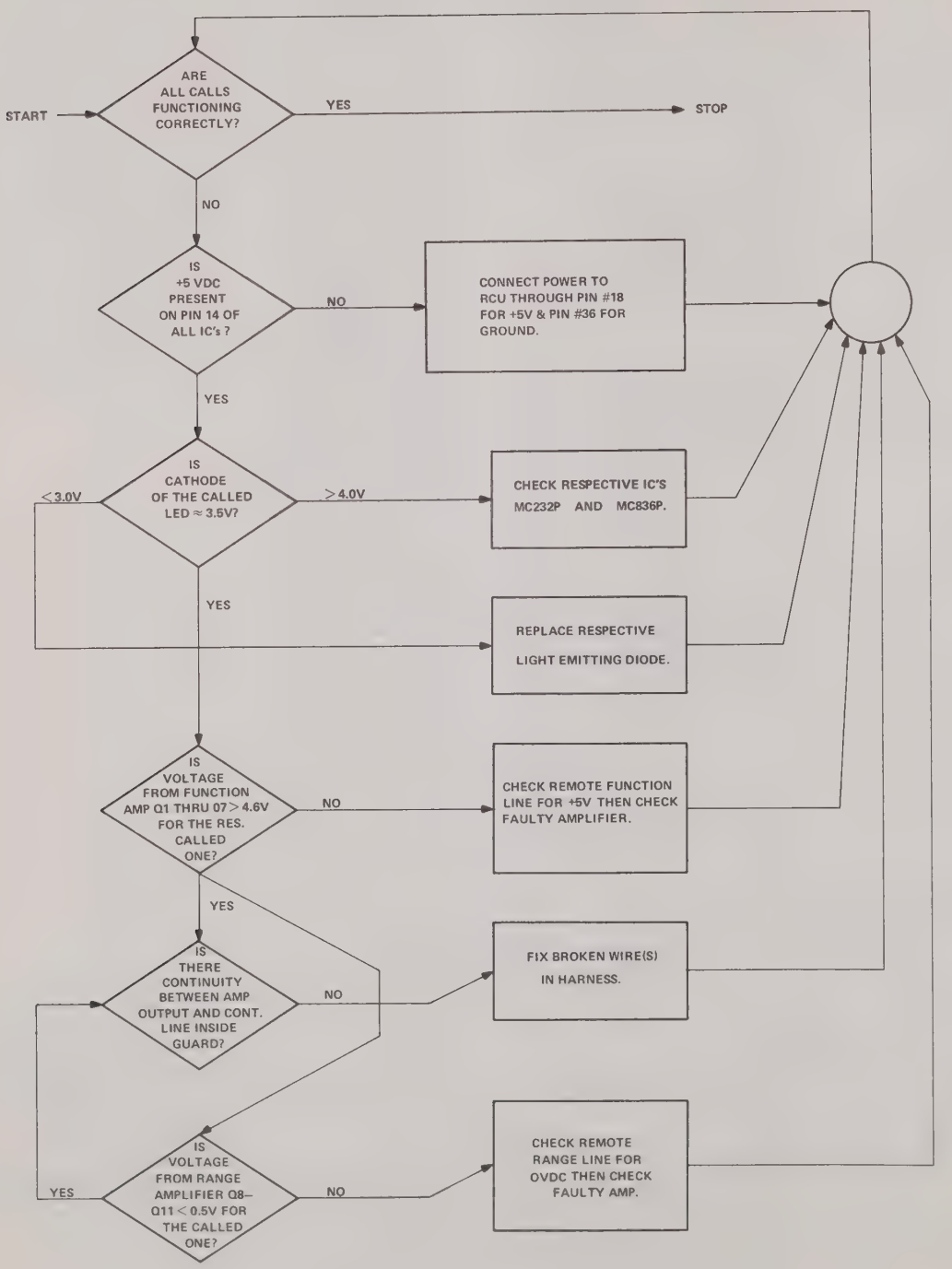

LEGEND:
DIAMONDS → DECISIONS
RECTANGLES → OPERATIONS
CIRCLES → LOOP RE-ENTRY
ABBREVIATIONS: LED - LIGHT EMITTING DIODES
START
ARE ALL CALLS FUNCTIONING CORRECTLY?
YES
STOP
NO
IS +5 VDC PRESENT ON PIN 14 OF ALL IC's ?
NO
CONNECT POWER TO RCU THROUGH PIN #18 FOR +5V & PIN #36 FOR GROUND.
YES
IS CATHODE OF THE CALLED LED ≈ 3.5V?
<3.0V
>4.0V
CHECK RESPECTIVE IC'S MC232P AND MC836P.
YES
REPLACE RESPECTIVE LIGHT EMITTING DIODE.
IS VOLTAGE FROM FUNCTION AMP Q1 THRU 07 > 4.6V FOR THE RES. CALLED ONE?
NO
CHECK REMOTE FUNCTION LINE FOR +5V THEN CHECK FAULTY AMPLIFIER.
YES
IS THERE CONTINUITY BETWEEN AMP OUTPUT AND CONT. LINE INSIDE GUARD?
NO
FIX BROKEN WIRE(S) IN HARNESS.
IS VOLTAGE FROM RANGE AMPLIFIER Q8–Q11 < 0.5V FOR THE CALLED ONE?
YES
NO
CHECK REMOTE RANGE LINE FOR OVDC THEN CHECK FAULTY AMP.

Figure 36.

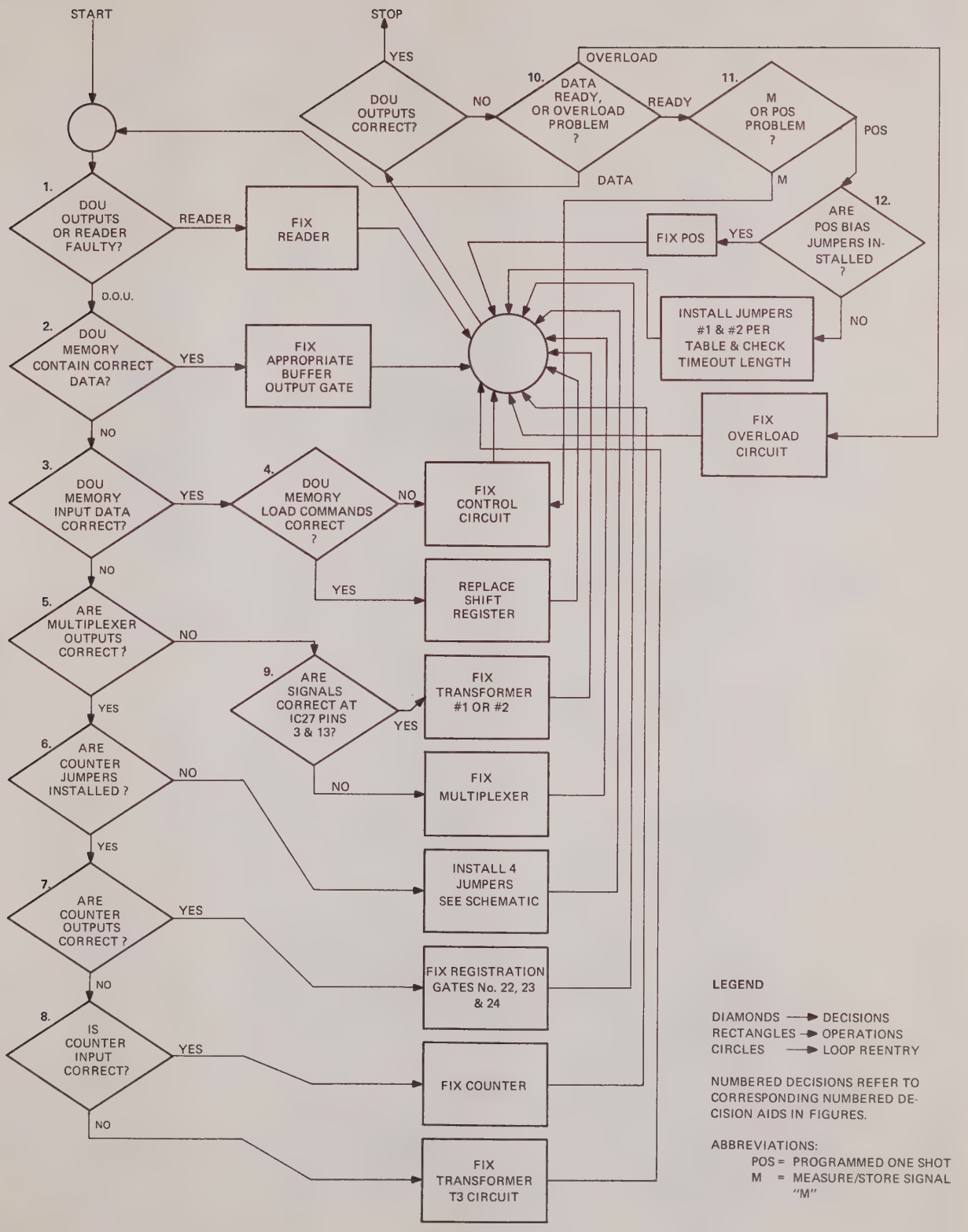


Figure 35. DECISION FLOW CHART –DOU TROUBLESHOOTING

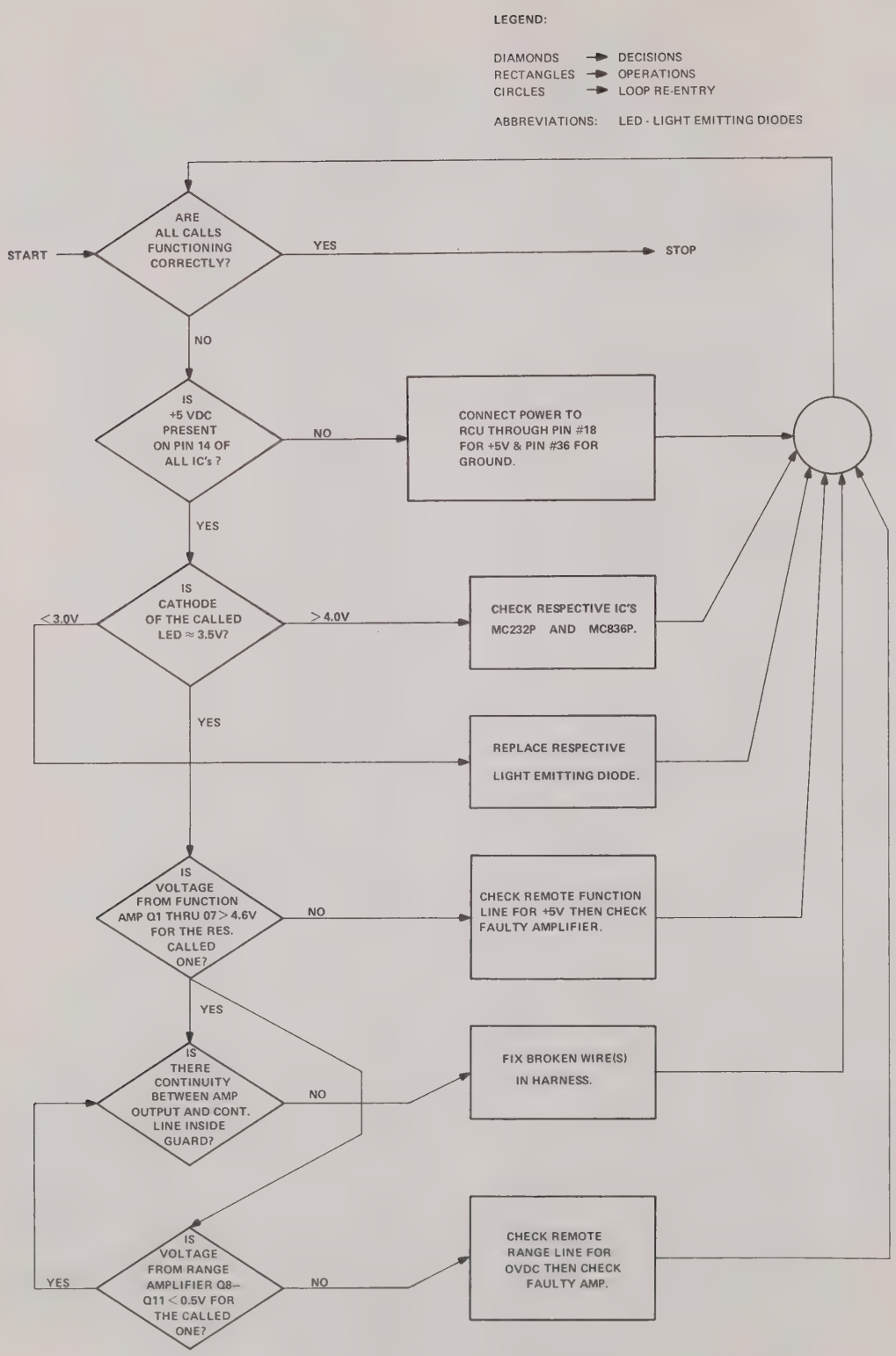

LEGEND:
DIAMONDS → DECISIONS
RECTANGLES → OPERATIONS
CIRCLES → LOOP RE-ENTRY
ABBREVIATIONS: LED - LIGHT EMITTING DIODES
START
ARE ALL CALLS FUNCTIONING CORRECTLY?
YES
STOP
NO
IS +5 VDC PRESENT ON PIN 14 OF ALL IC's ?
NO
CONNECT POWER TO RCU THROUGH PIN #18 FOR +5V & PIN #36 FOR GROUND.
YES
IS CATHODE OF THE CALLED LED ≈ 3.5V?
< 3.0V
> 4.0V
CHECK RESPECTIVE IC'S MC232P AND MC836P.
YES
REPLACE RESPECTIVE LIGHT EMITTING DIODE.
IS VOLTAGE FROM FUNCTION AMP Q1 THRU 07 > 4.6V FOR THE RES. CALLED ONE?
NO
CHECK REMOTE FUNCTION LINE FOR +5V THEN CHECK FAULTY AMPLIFIER.
YES
IS THERE CONTINUITY BETWEEN AMP OUTPUT AND CONT. LINE INSIDE GUARD?
NO
FIX BROKEN WIRE(S) IN HARNESS.
IS VOLTAGE FROM RANGE AMPLIFIER Q8–Q11 < 0.5V FOR THE CALLED ONE?
YES
NO
CHECK REMOTE RANGE LINE FOR OVDC THEN CHECK FAULTY AMP.

Figure 36.

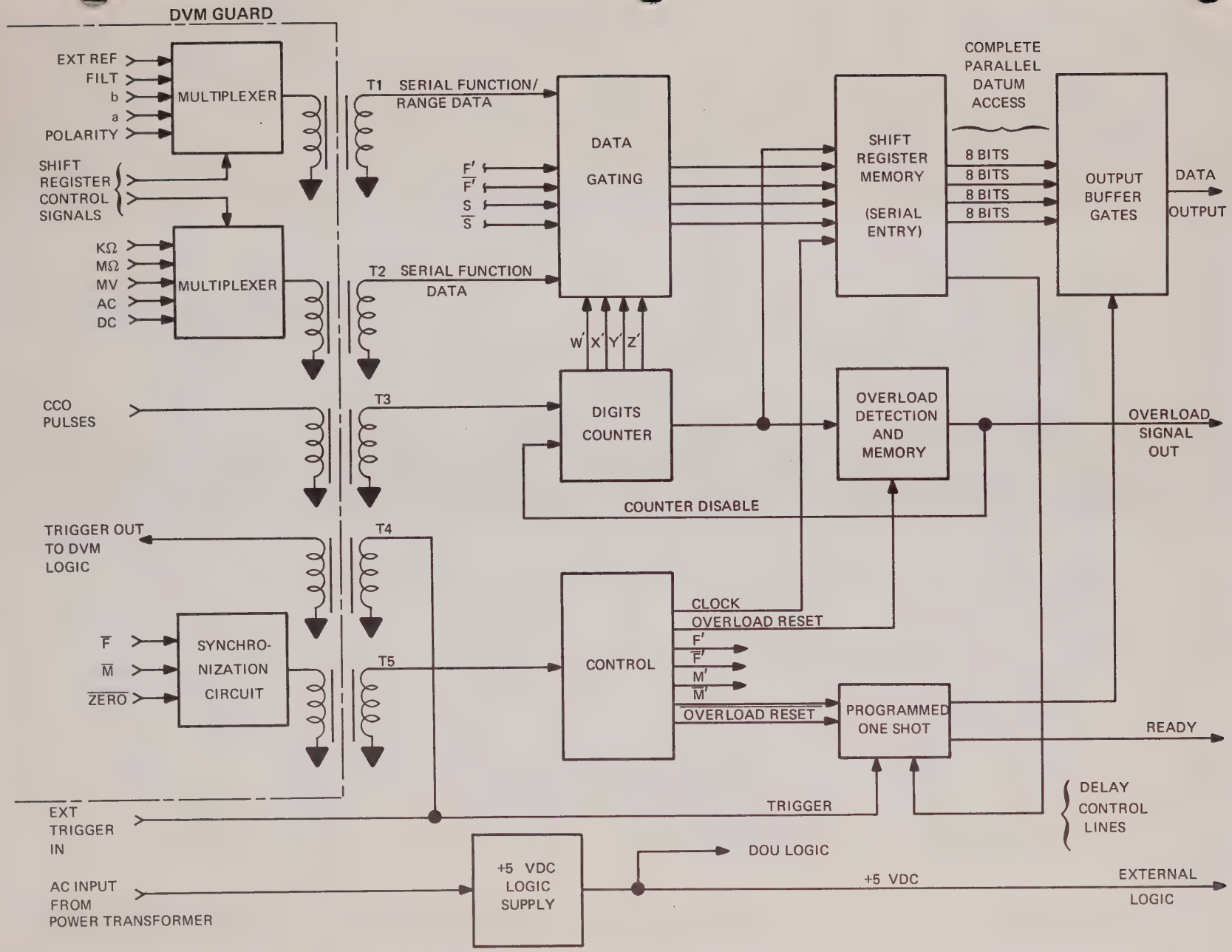
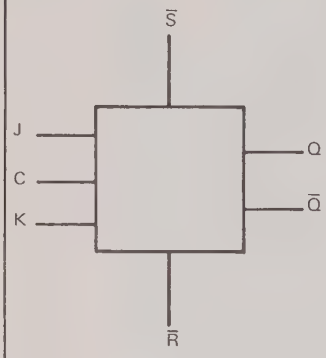
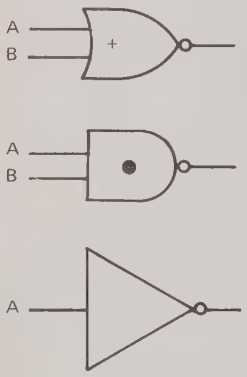


Figure 39. DATA OUTPUT UNIT BLOCK DIAGRAM

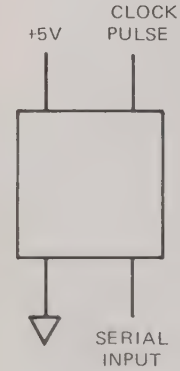
<table>
<tr><th>LOGIC SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td> 
</td><td>J-K Flip Flop</td><td>Operation of the J-K flip flop is shown by the following truth tables. Note that "S" and "R" inputs are dominant over "J" and "K" inputs.

J | K | Q_{n+1}
0 | 0 | Q_n
0 | 1 | 0
1 | 0 | 1
1 | 1 | $\overline{Q}_n$

S | R | Q $\overline{Q}$
0 | 0 | Undefined
0 | 1 | 1 0 Set
1 | 0 | 0 1 Reset
1 | 1 | Normal Condition</td></tr>
<tr><td> 
</td><td>NOR Gate

NAND Gate

Inverter</td><td>The following table shows gate and inverter operation, Although only two-input gates are shown, operation is identical for gates having additional inputs.

A | B | NOR | NAND | INVERTER
0 | 0 | 1 | 1 | 1
0 | 1 | 1 | 1 | 1
1 | 0 | 0 | 1 | 0
1 | 1 | 0 | 0 | 0</td></tr>
<tr><td> 
</td><td>Shift Register</td><td>Four 8-bit, serial-in parallel-out shift registers are used. A logical "1" at the input enters a logical "1" into the register. The register output terminals are not shown on the schematic; however, they are given in the following table:

Shift Register Outputs
Q1 | 3
Q2 | 4
Q3 | 5
Q4 | 6
Q5 | 10
Q6 | 11
Q7 | 12
Q8 | 13</td></tr>
</table>

Figure 40. EXPLANATION OF LOGIC SYMBOLOGY USED IN DOU

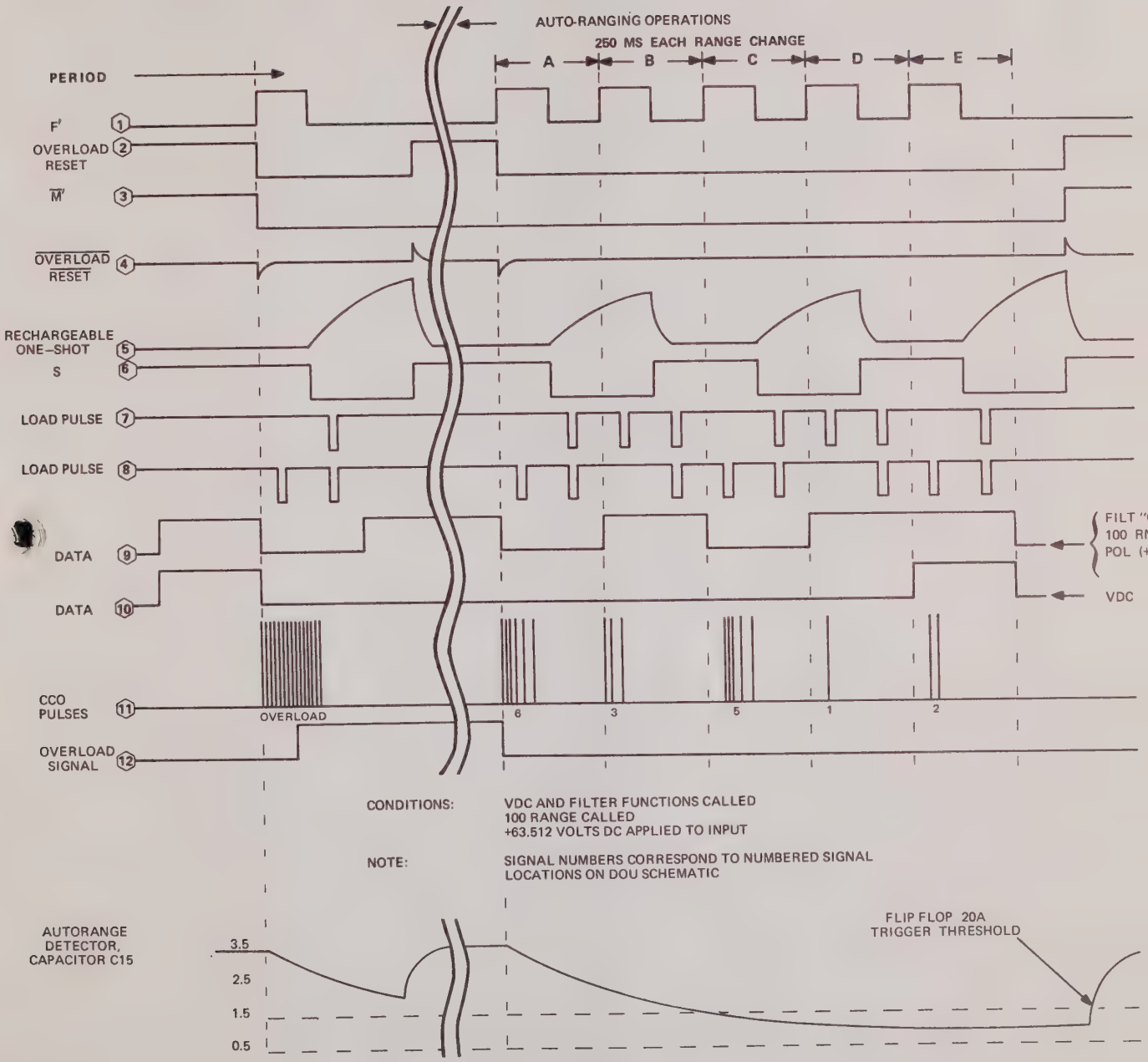
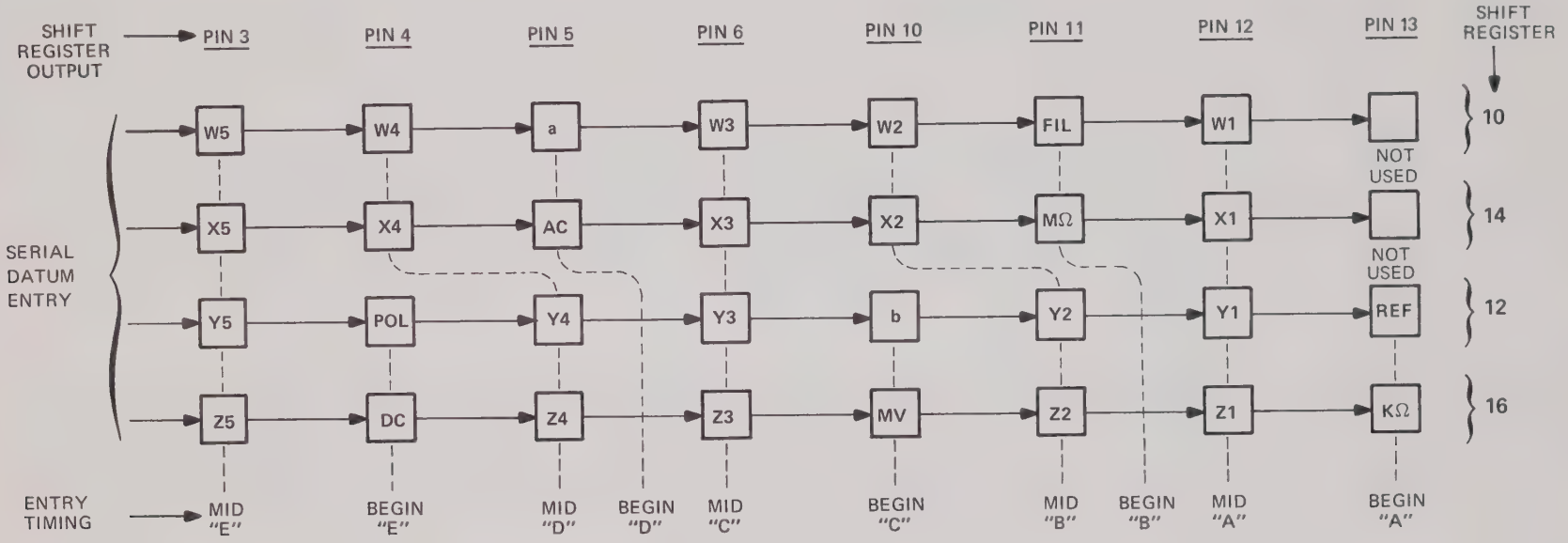


Figure 41. DOU TIMING DIAGRAM



LEGEND: 1. ☐ DENOTES FUNCTION, RANGE, OR DIGIT BIT
2. ENTRY TIMING DESIGNATIONS DENOTE WHEN DATA IS LOADED

Figure 42. SHIFT REGISTER LOAD SEQUENCE (Data Output Unit)

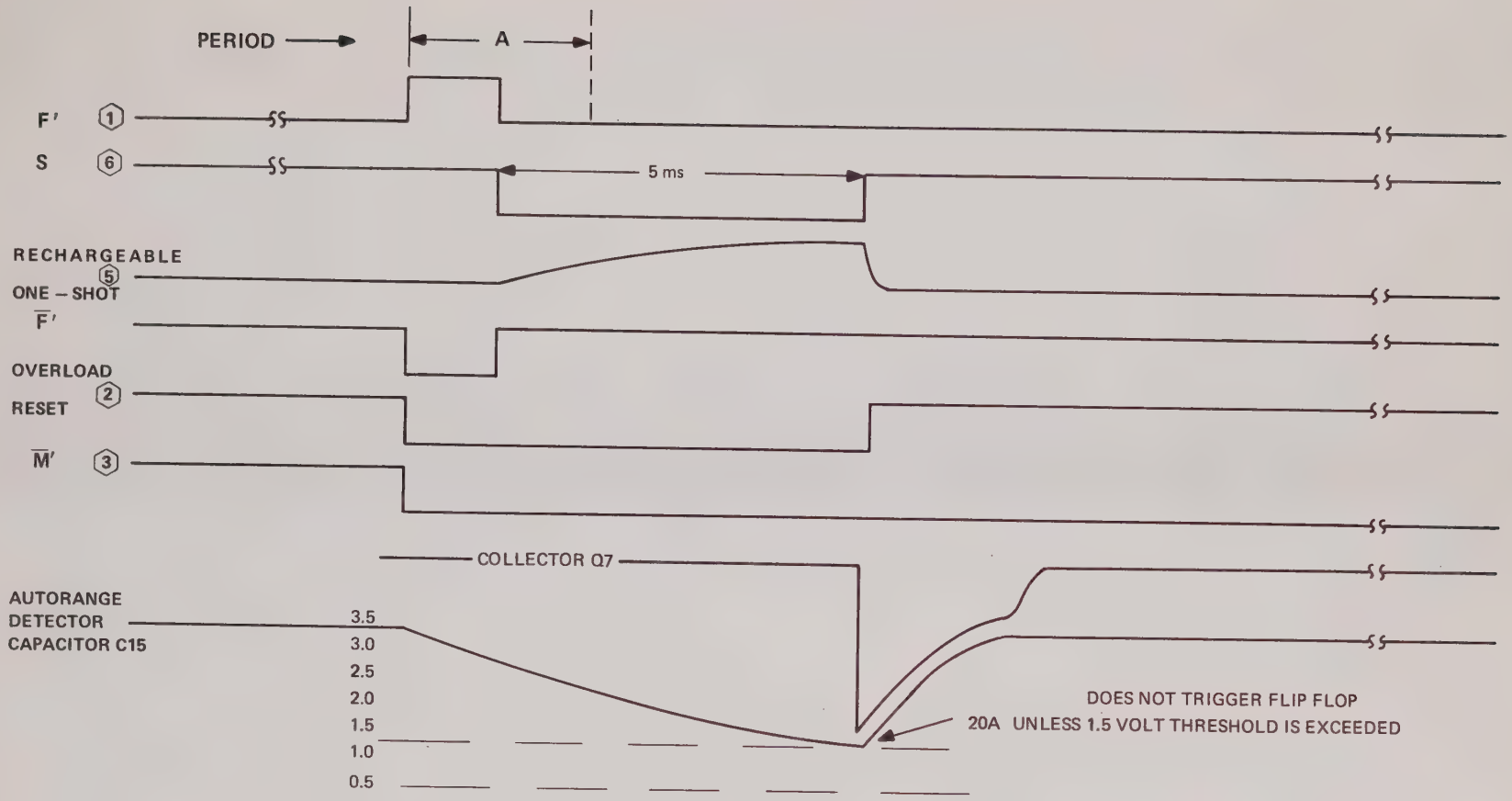


Figure 43. CONTROL SIGNAL TIMING DURING AUTORANGE

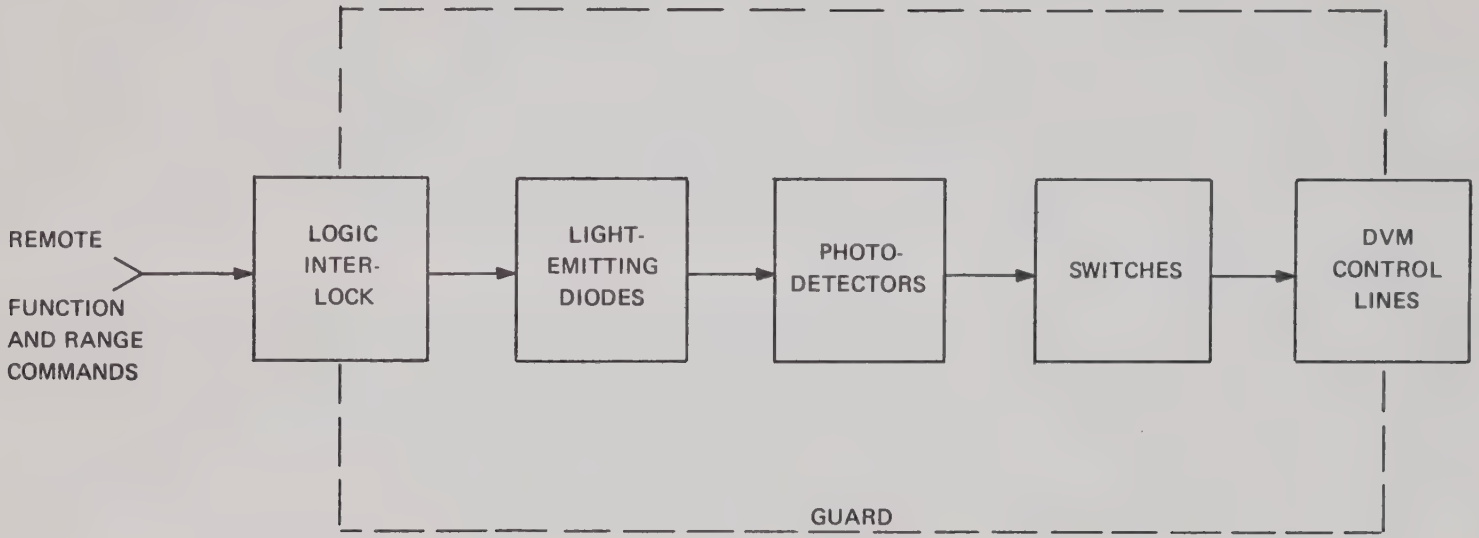
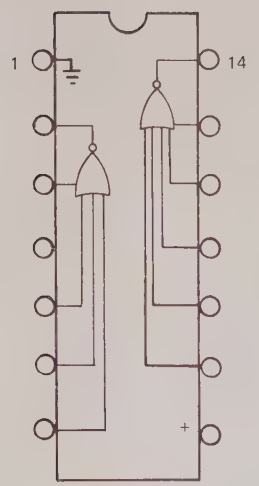
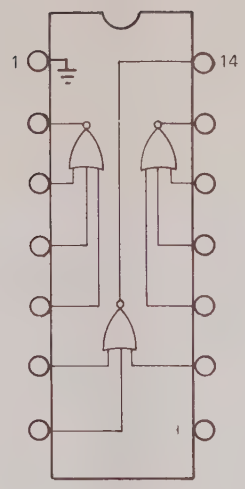


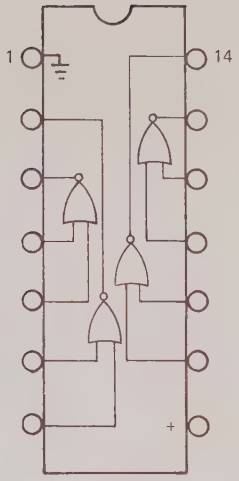
Figure 44. REMOTE CONTROL UNIT BLOCK DIAGRAM



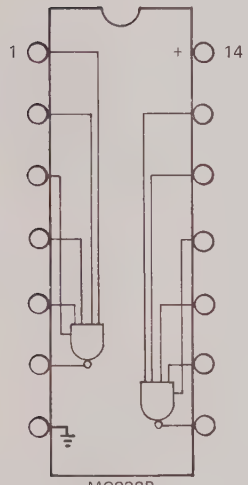
SP317A
JF268557



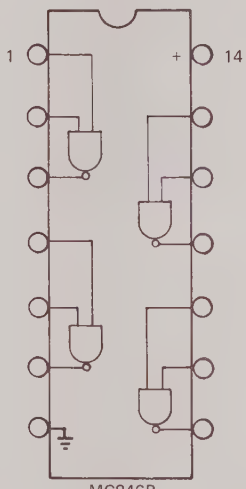
SP370A
JF268565



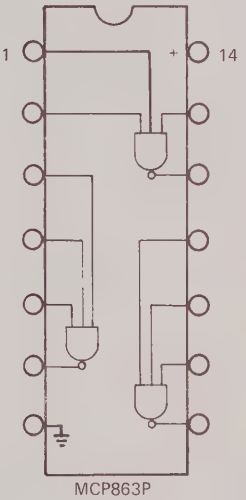
SP380A
JF268540



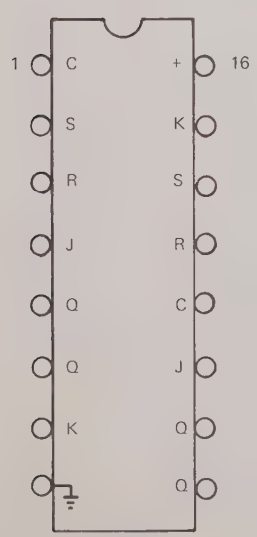
MC832P
JF268383



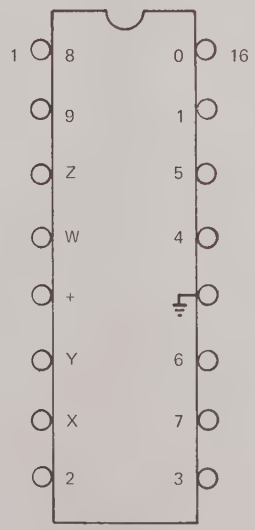
MC846P
JF268375



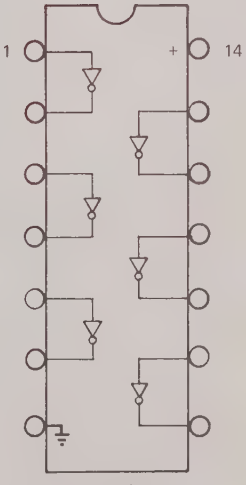
MCP863P
JF266312



SP322B
JF268441



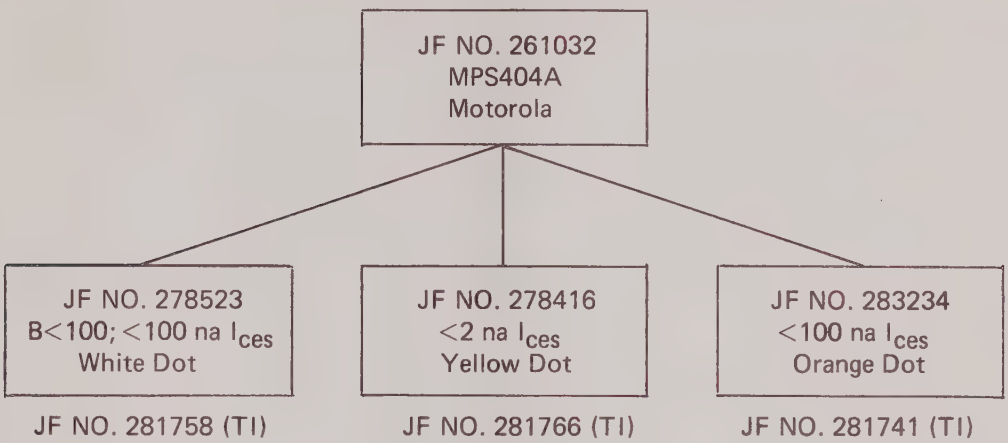
DM8840N
JF267211



836P
JF268367

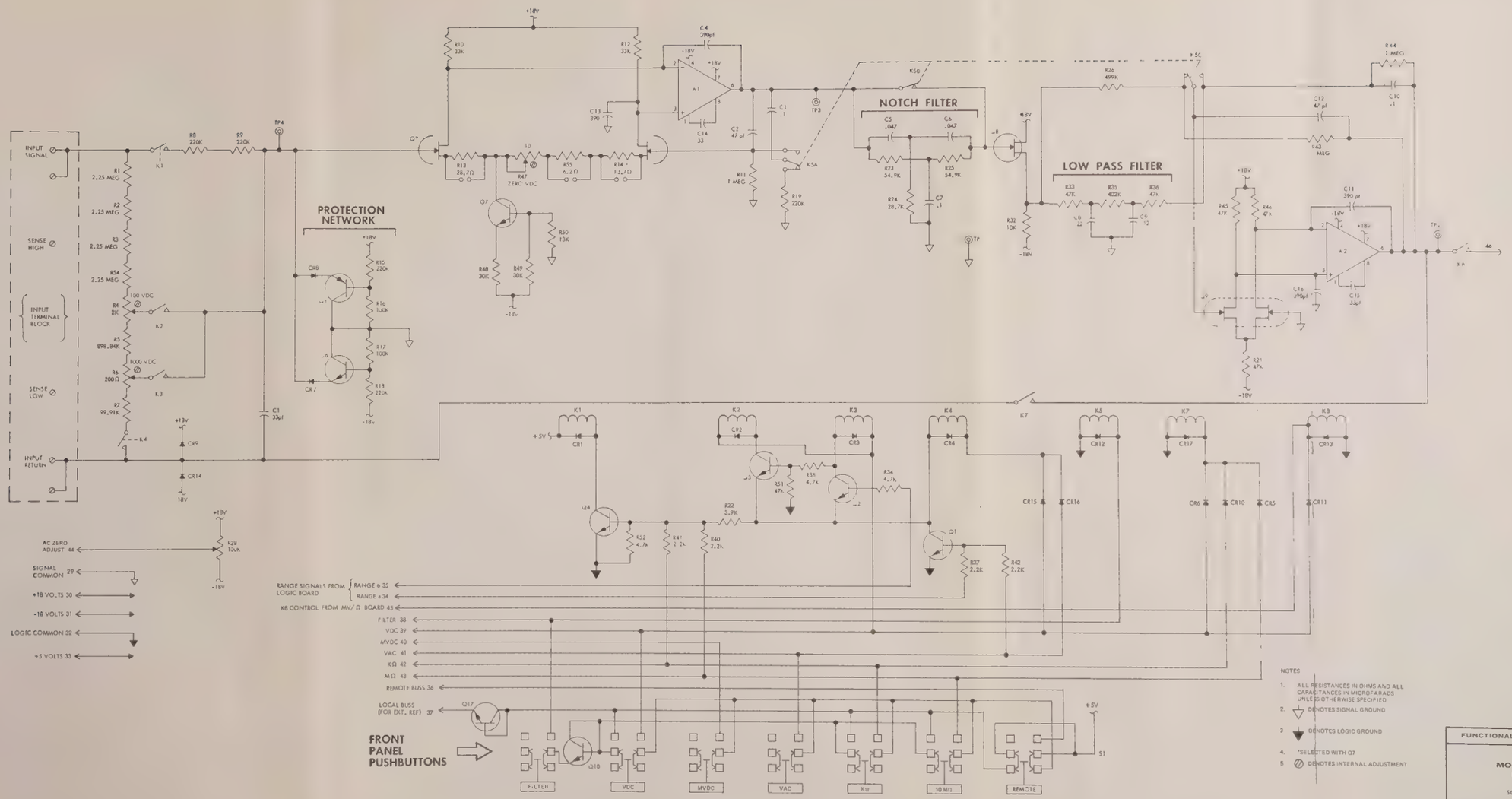
TOP VIEW

8100A/8300A SELECTED TRANSISTORS



The above selected part numbers are used in the following areas of the 8100 and 8300.

8100A (8)		8300A (6)	
Schematic Designation	Color	Schematic Designation	Color
Q19	White	Q106	Orange
Q20	White	Q107	Orange
Q21	White	Q116	Orange
Q22	White	Q123	Orange
Q23	White		
Q25	Orange	MV/Ω Converter	
Q61	Yellow	Q6	Orange
Q76	Yellow	Q7	Orange



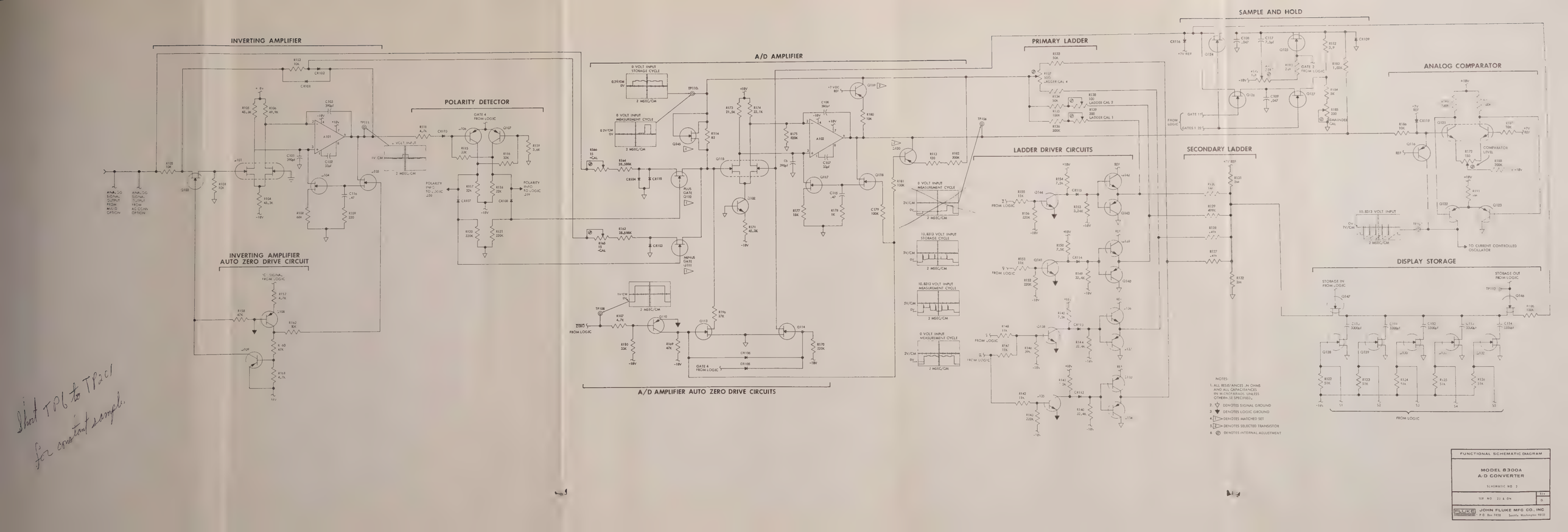
FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
BUFFER

SCHEMATIC NO

SER NO 133 & ON | REV 1

JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



Short TP6 to TP21 for constant sample.

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
A/D CONVERTER

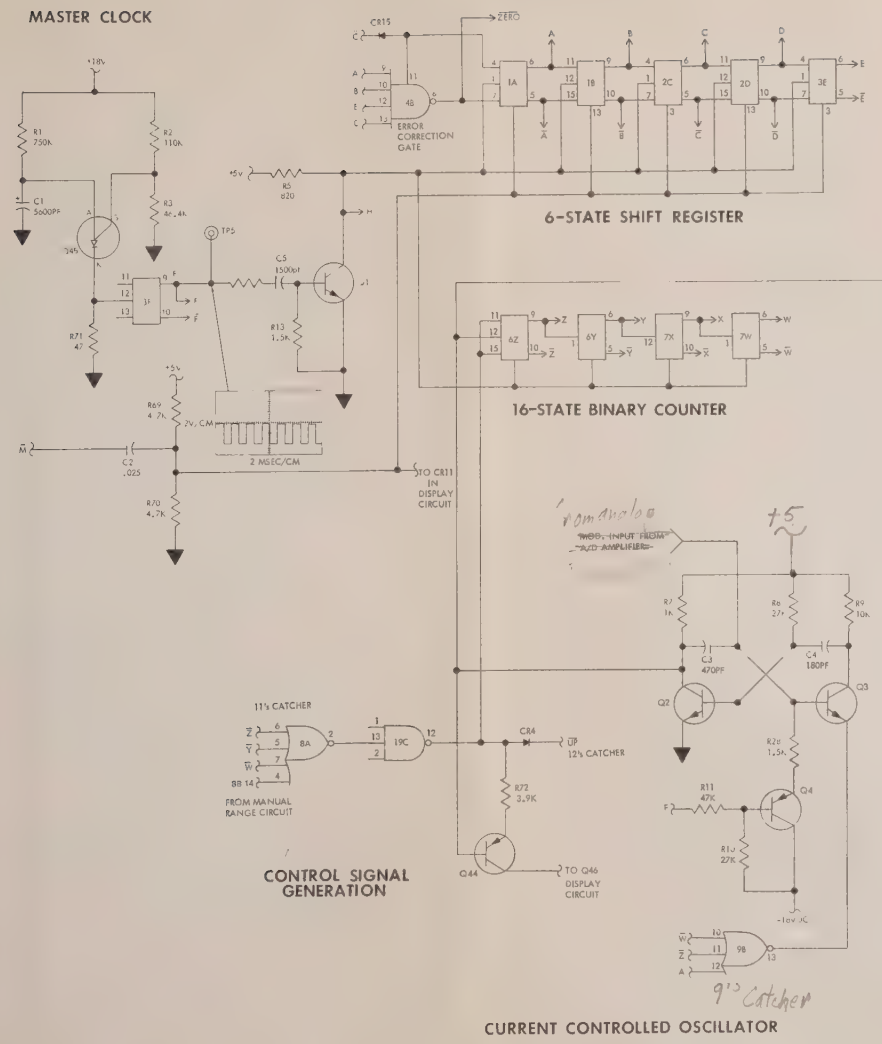
SCHEMATIC NO. 2

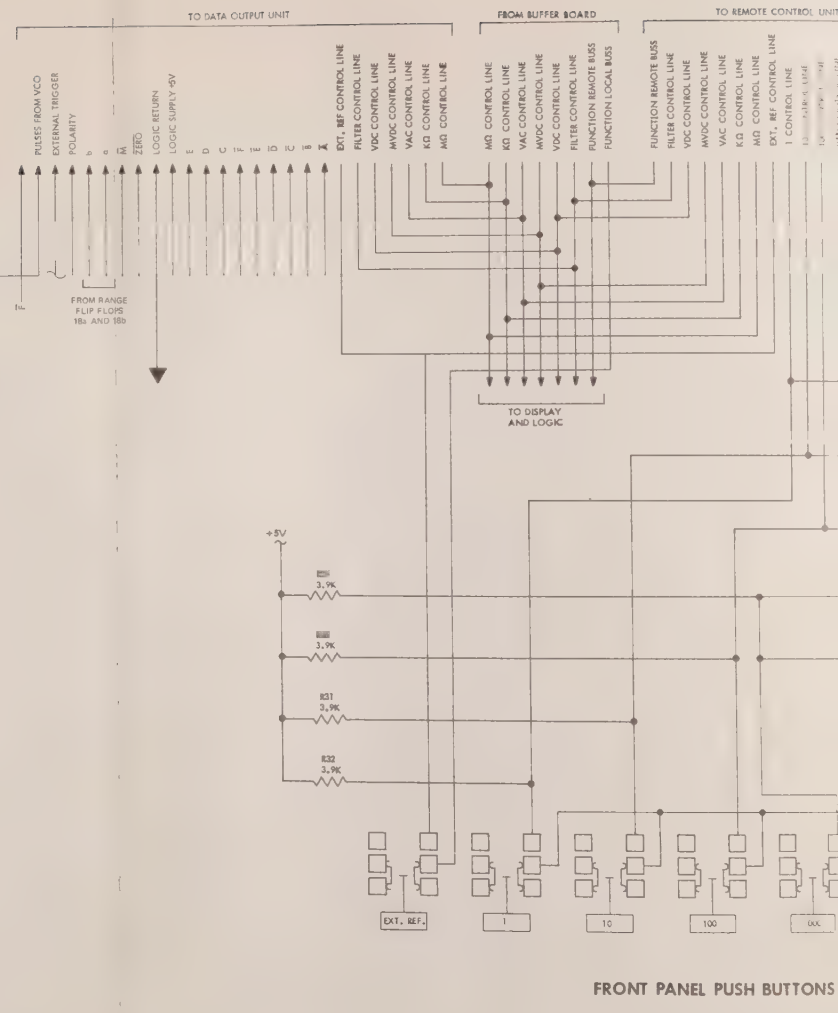
SEE NO. 22 & ON

A2

9

JOHN FLUKE MFG CO., INC
P.O. Box 7428 Seattle, Washington 98133


MASTER CLOCK
ERROR CORRECTION GATE
6-STATE SHIFT REGISTER
16-STATE BINARY COUNTER
TO CR11 IN DISPLAY CIRCUIT
11% CATCHER
FROM MANUAL RANGE CIRCUIT
CONTROL SIGNAL GENERATION
TO Q46 DISPLAY CIRCUIT
CURRENT CONTROLLED OSCILLATOR


TO DATA OUTPUT UNIT
FROM BUFFER BOARD
TO REMOTE CONTROL UNIT
PULSES FROM VCO
EXTERNAL TRIGGER
POLARITY
ZERO
LOGIC RETURN
LOGIC SUPPLY +5V
FROM RANGE FLIP FLOPS 18a AND 18b
TO DISPLAY AND LOGIC
FRONT PANEL PUSH BUTTONS
EXT. REF.

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ▽ DENOTES SIGNAL COMMON
4. ⊕ DENOTES INTERNAL ADJUSTMENT

-18V INPUT FROM POWER SUPPLY → 18

+18V INPUT FROM POWER SUPPLY → 16

REFERENCE VOLTAGE FROM LADDER SEE A/D SCHEMATIC → 12

11 LOGIC COMMON

15 SIGNAL COMMON

5 KΩ CONTROL LINE

14 MV CONTROL LINE

1 RANGE b' CONTROL

4 KΩ CONTROL LINE

2 RANGE a' CONTROL

13 MV CONTROL LINE

6 K8 CONTROL LINE

9 MΩ CONTROL LINE

10 MΩ CONTROL LINE

C5 1 · R11 1M · TP1 · .02V/CM · .5 MSEC/CM · +18V · R10 1M · Q3 · C6 33PF · A1 · C17 10PF · R9 22K · R13 2.2M · C7 10PF · R14 3.9K · C8 .47 · CR5 · CR6 · C11 · TP2 · R15 49.9K · R16 49.9K · C12 33PF · K2 · 7 OUTPUT TO A/D CONVERTER · C9 .22 · Q4 · R17 100K · C10 0.22 · TP3 · 100M R18 · 17 MV ZERO ADJUST SEE A/D SCHEMATIC · C16 0.01 · R32 500 · R60 510Ω · R28 50 Ω · R30 90K · R31 899.73K · 100 MV · 1000 MV · K8 · R21 1M · C13 .047 · R29 9.9975K

2V/CM · 0.5 MSEC/CM · TP4 · TO Q1 GATE · -18V · R35 39K · R33 390K · R36 390K · R34 10K · C15 5000PF · C14 3900PF · R37 39K · Q7 · Q6

MULTIVIBRATOR

CR11 · Q8 · R51 390 · CR12 · Q9 · CR18 · CR13 K7 · CR14 K6 · CR15 K4 · CR16 K5 · CR19 K2 · CR20 K1 · CR22 K8 · R48 3.9K · R49 3.9K · R52 3.9K · R50 3.9K · R53 3.9K · R55 22K · Q10 · CR21 · CR23 · R54 3.9K · CR24 · CR25 K3 · TP5

RELAY DRIVERS

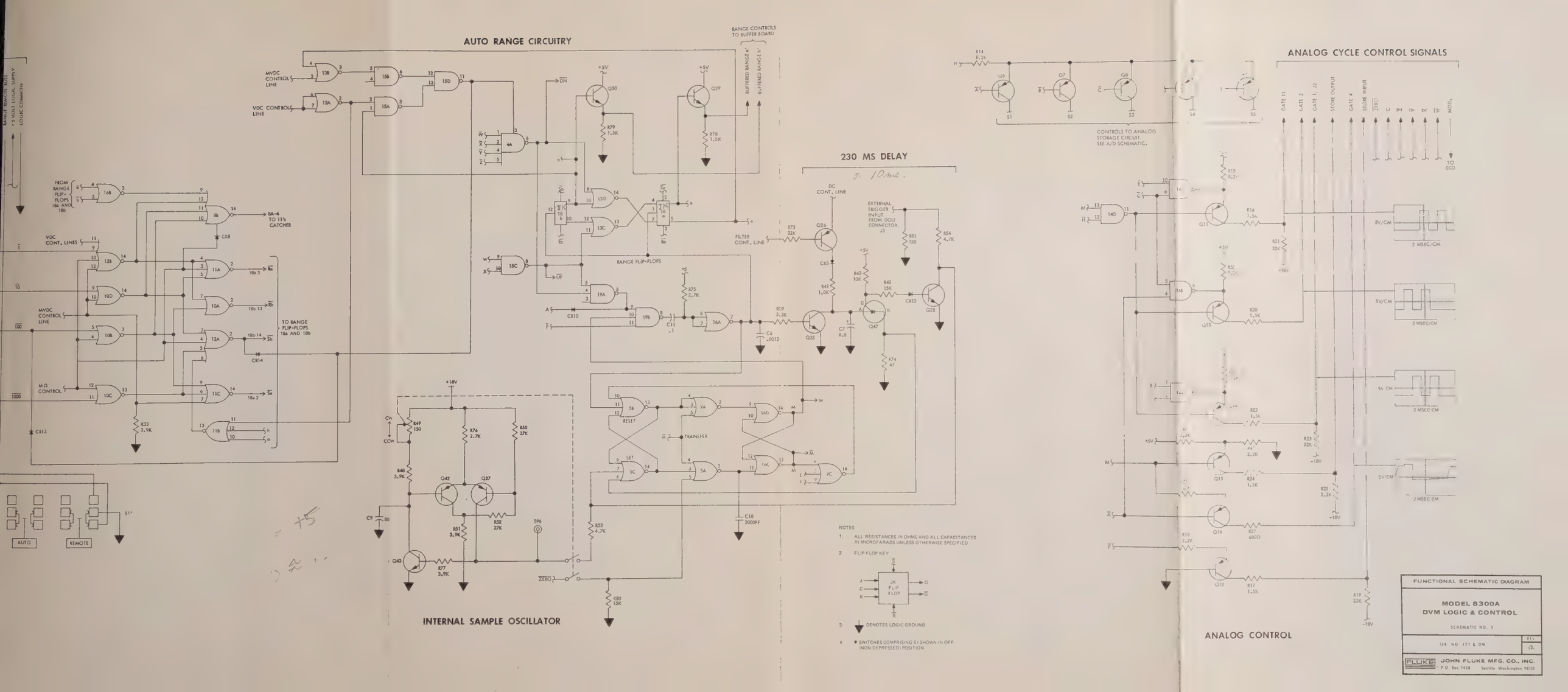
FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
MILLIVOLTS/OHMS CONVERTER

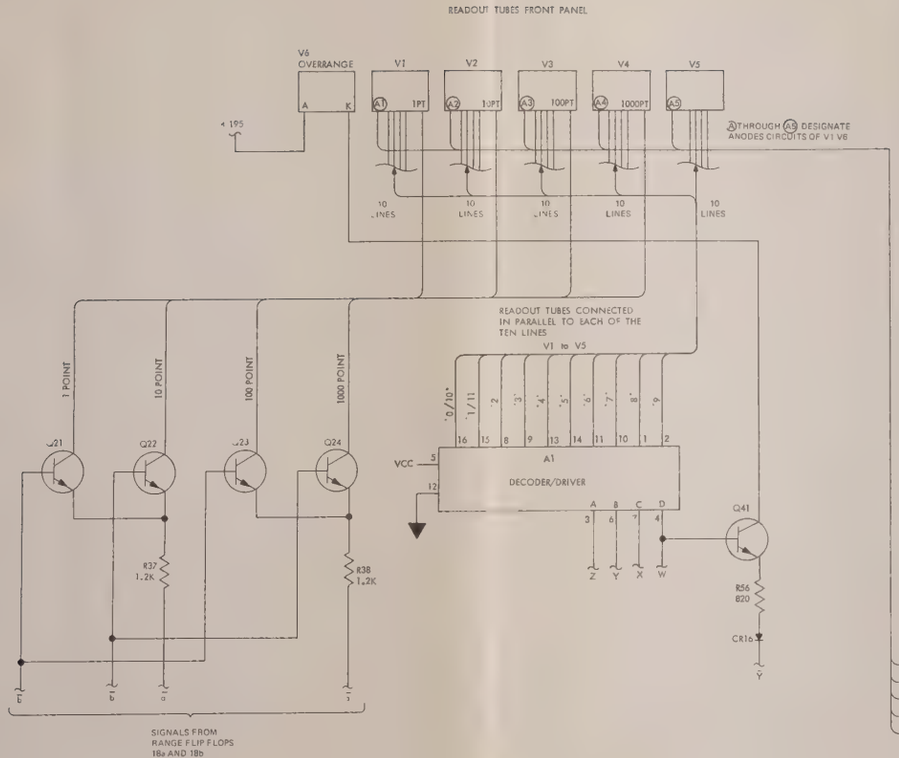
SCHEMATIC NO. 7

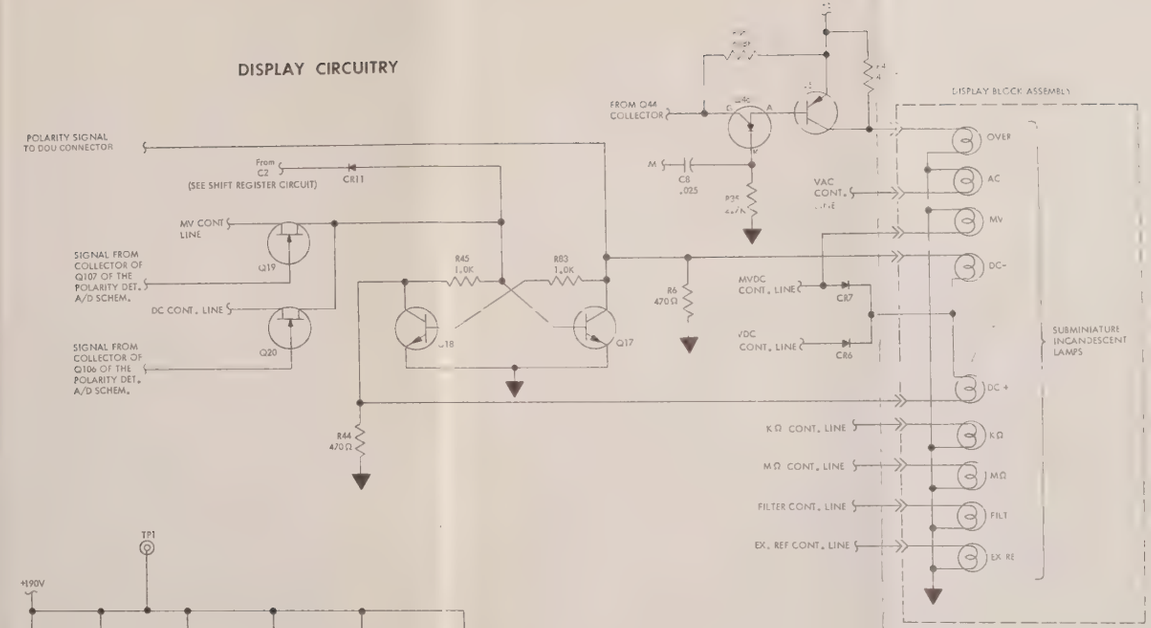
SER NO. 123 & ON · REV a

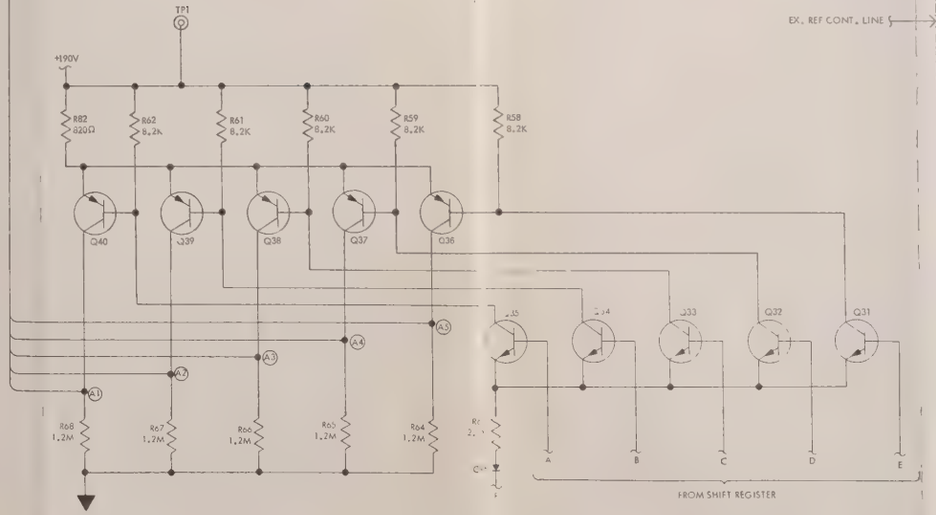
FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


AUTO RANGE CIRCUITRY
RANGE CONTROLS TO BUFFER BOARD
MVDC CONTROL LINE
VDC CONTROL LINE
BUFFERED RANGE a
BUFFERED RANGE b
230 MS DELAY
RANGE FLIP-FLOPS
FILTER CONT. LINE
DC CONT. LINE
EXTERNAL TRIGGER INPUT FROM DOU CONNECTOR J3
FROM RANGE FLIP-FLOPS 18a AND 18b
TO 13% CATCHER
VDC CONT. LINES
MVDC CONTROL LINE
MΩ CONTROL
TO RANGE FLIP-FLOPS 18a AND 18b
RANGE REMOTE BUS
+5 VOLT LOGIC SUPPLY
LOGIC COMMON
AUTO
REMOTE
INTERNAL SAMPLE OSCILLATOR
TRANSFER
RESET
SET
ZERO
CW
CCW
NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2 FLIP FLOP KEY
3. DENOTES LOGIC GROUND
4. ◆ SWITCHES COMPRISING S1 SHOWN IN OFF (NON DEPRESSED) POSITION
CONTROLS TO ANALOG STORAGE CIRCUIT SEE A/D SCHEMATIC.
ANALOG CYCLE CONTROL SIGNALS
GATE 11
GATE 2
GATE 1, 12
STORE OUTPUT
GATE 4
STORE INPUT
ZERO
MODE
TO CCD
2 MSEC/CM
ANALOG CONTROL
FUNCTIONAL SCHEMATIC DIAGRAM
MODEL 8300A
DVM LOGIC & CONTROL
SCHEMATIC NO. 3
SER NO 123 & ON
JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle Washington 98133

DISPLAY CIRCUITRY



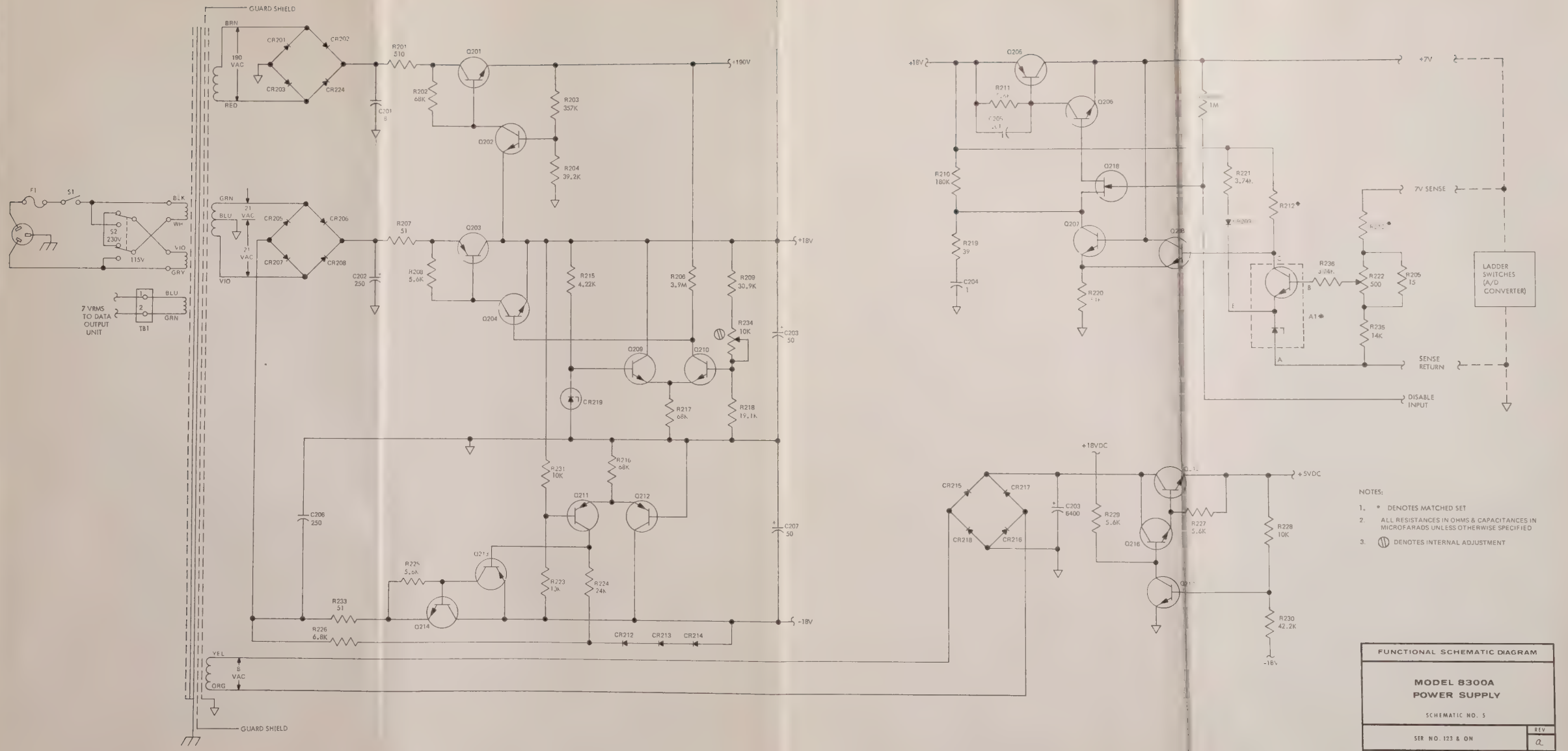




ANODE STROBING CONTROL

NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC GROUND

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DISPLAY	
SCHEMATIC NO 4	
SER NO 123 & ON	REV A
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle Washington 98133	



NOTES:

1. * DENOTES MATCHED SET
2. ALL RESISTANCES IN OHMS & CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
3. ⓘ DENOTES INTERNAL ADJUSTMENT

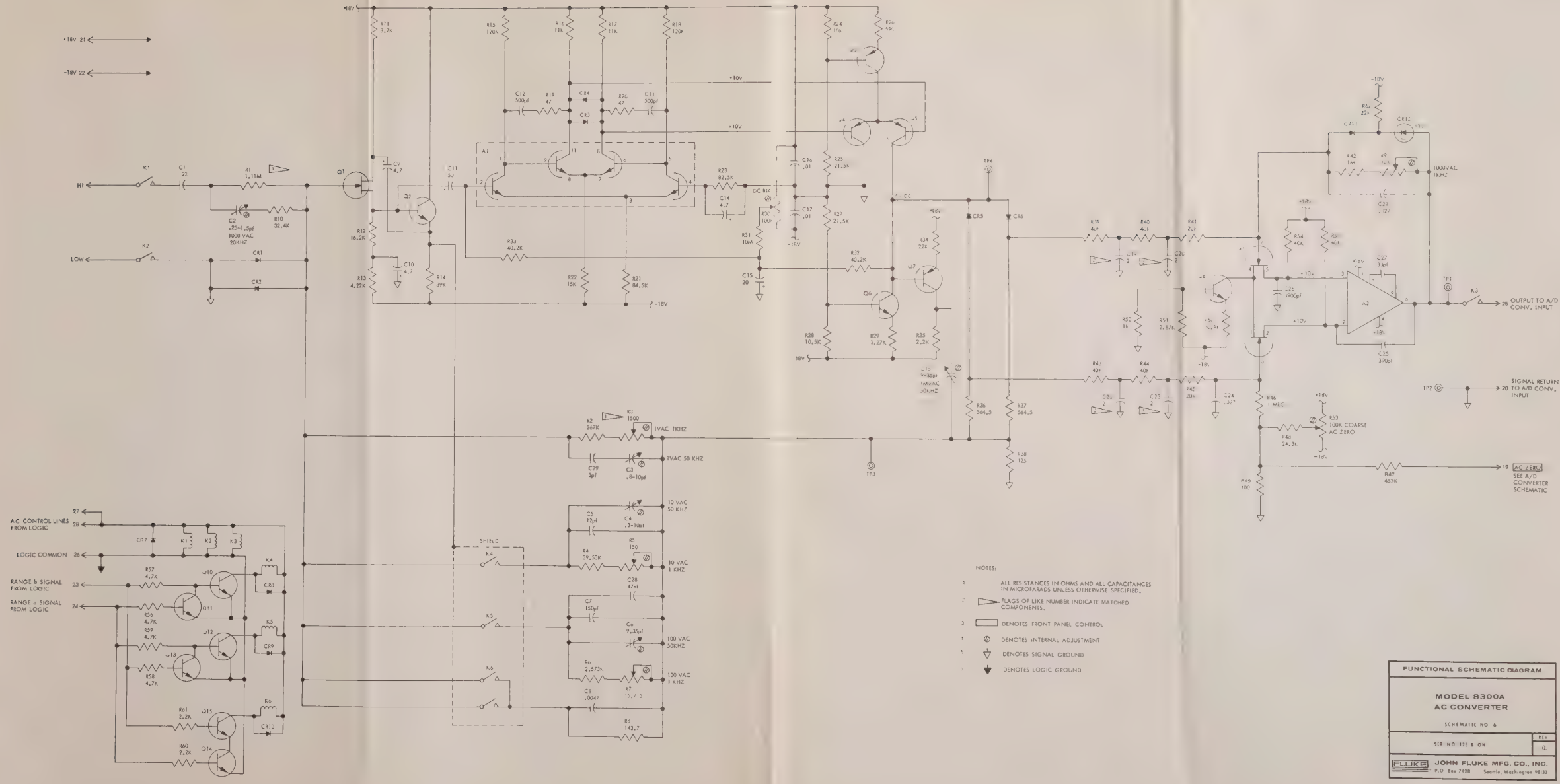
FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A POWER SUPPLY

SCHEMATIC NO. 5

SER NO. 123 & ON | REV a

FLUKE JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle, Washington 98133



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLAGS OF LIKE NUMBER INDICATE MATCHED COMPONENTS.
3. DENOTES FRONT PANEL CONTROL
4. DENOTES INTERNAL ADJUSTMENT
5. DENOTES SIGNAL GROUND
6. DENOTES LOGIC GROUND

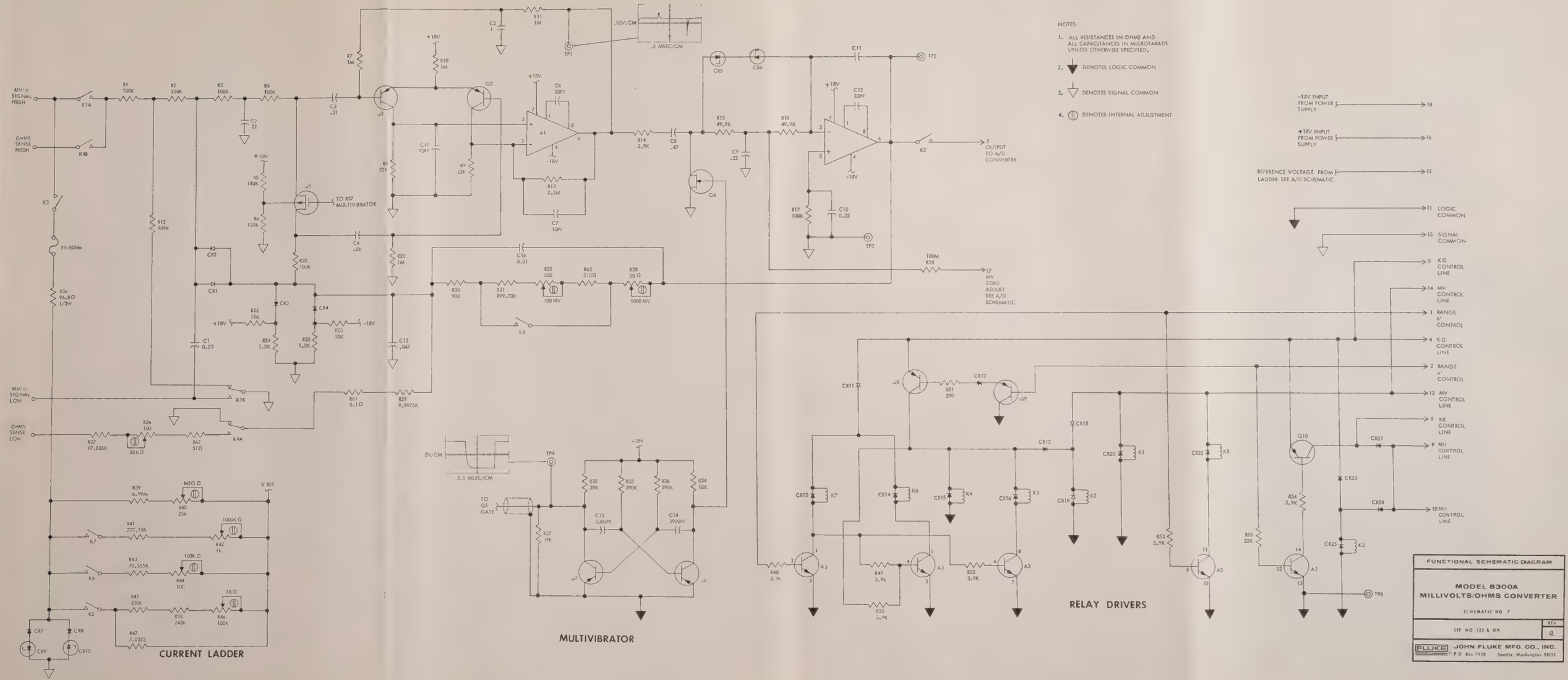
FUNCTIONAL SCHEMATIC DIAGRAM

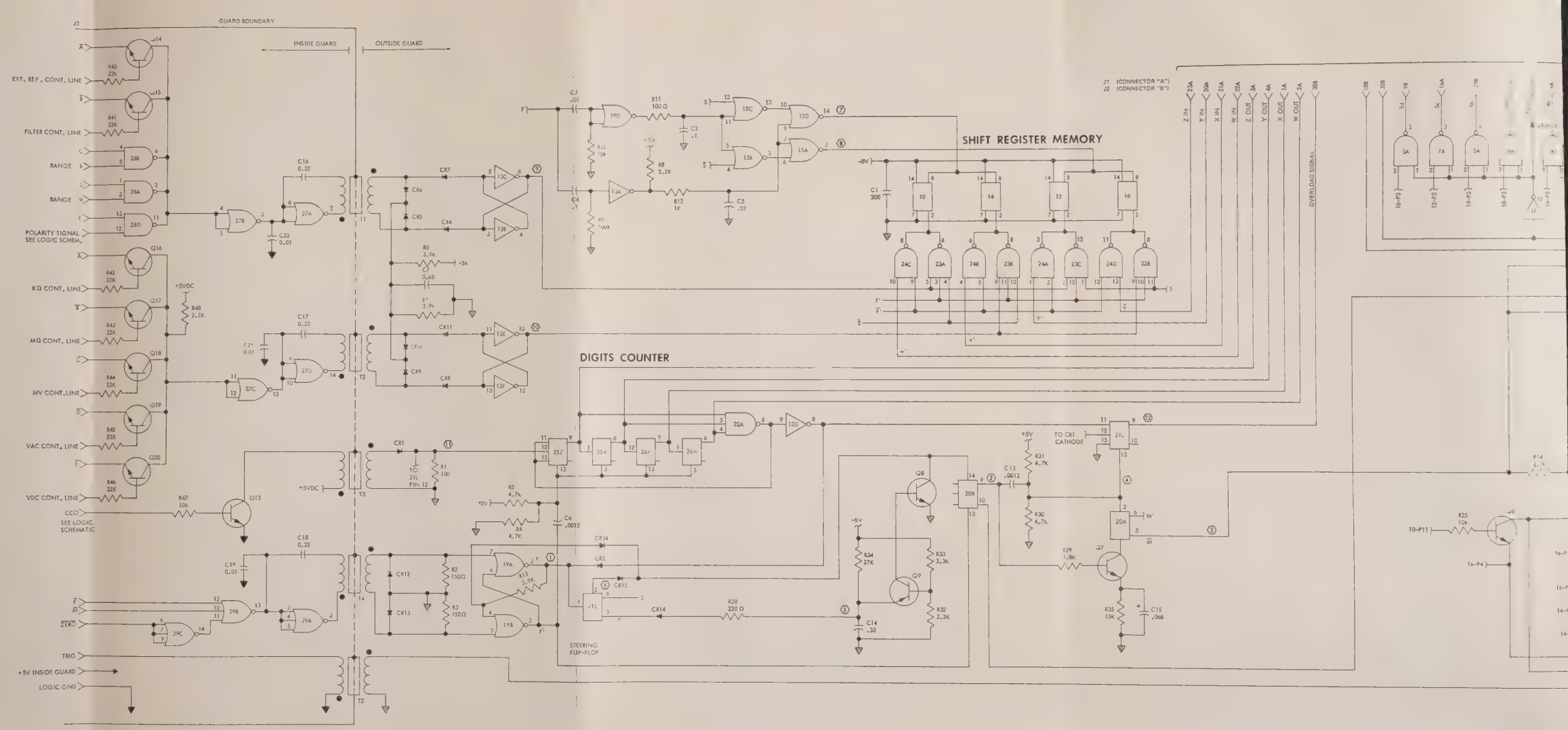
MODEL 8300A
AC CONVERTER

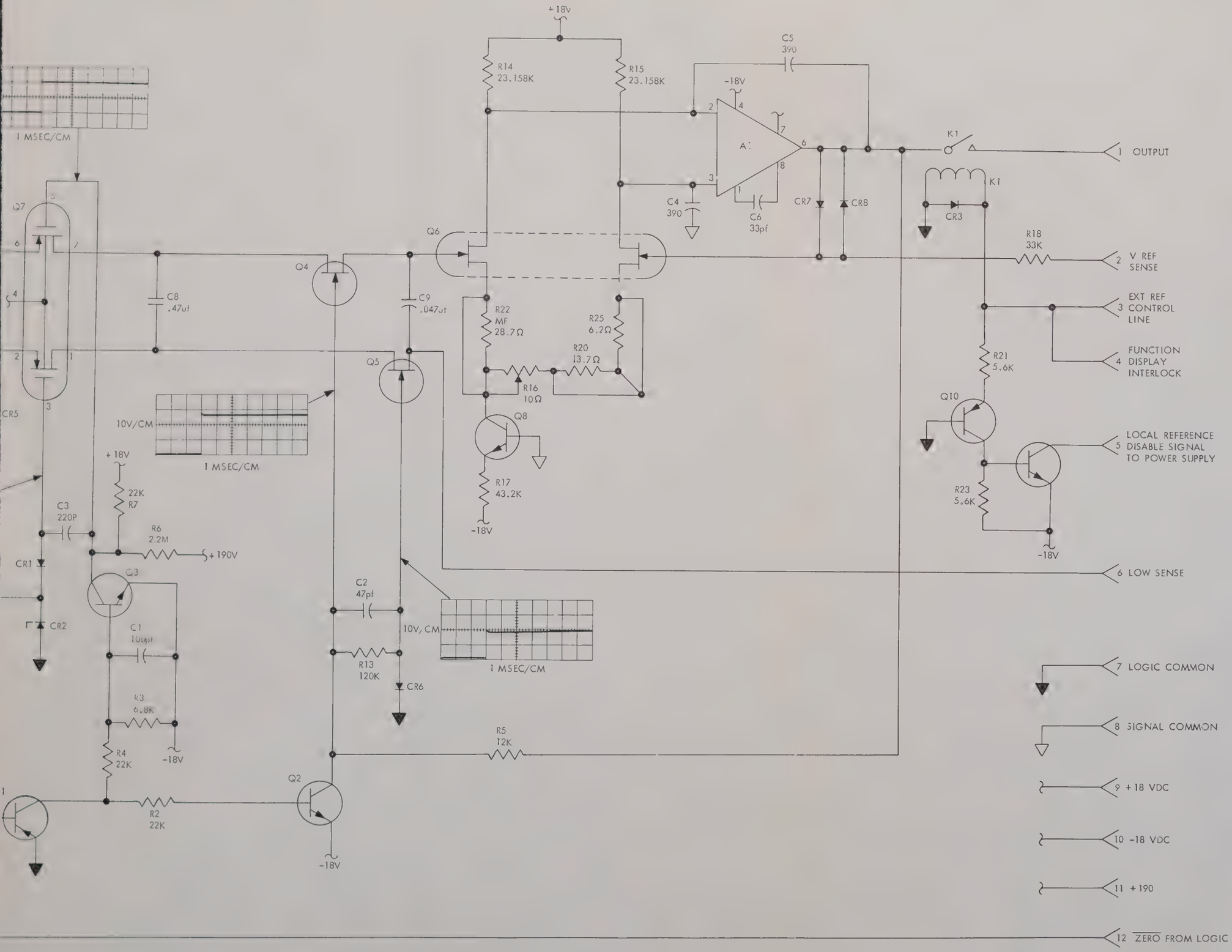
SCHEMATIC NO 6

SER NO 123 & ON	REV
	A

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. DENOTES LOGIC COMMON
3. DENOTES SIGNAL COMMON
4. DENOTES INTERNAL ADJUSTMENT
MV/Ω SIGNAL HIGH
OHMS SENSE HIGH
MV/Ω SIGNAL LOW
OHMS SENSE LOW
K1A
K4B
K4A
K1B
K2
K3
K8
R1 100K
R2 100K
R3 100K
R4 100K
C2 22
C3 .01
R7 1M
R10 1M
C5 1
TP1
.02V/CM
.5 MSEC/CM
+18V
Q3
C6 33PF
A1
C17 10PF
R8 22K
R9 22K
R14 3.9K
C8 .47
R5 49.9K
R16 49.9K
C9 .22
C11
TP2
CR5
CR6
C12 33PF
R17 100K
C10 0.22
TP3
7 OUTPUT TO A/D CONVERTER
R13 2.2M
C7 10PF
R5 180K
R6 120K
Q1
TO R37 MULTIVIBRATOR
C4 .01
R12 909K
R21 1M
R20 100K
CR2
CR1
C16 0.01
R30 90K
R31 899.73K
R32 500
100 MV
R60 510Ω
R28 50Ω
1000 MV
100M R18
17 MV ZERO ADJUST SEE A/D SCHEMATIC
F1-50Ma
R3a 96.8Ω 1/2W
R22 15K
CR3
CR4
R23 15K
R24 1.2K
R25 1.2K
C1 0.22
C13 .047
R61 5.1Ω
R29 9.9975K
R26 100
R27 97.835K
10 KΩ
R62 51Ω
2V/CM
0.5 MSEC/CM
TP4
TO Q1 GATE
R35 39K
R33 390K
R36 390K
R34 10K
C15 5000PF
C14 3900PF
R37 19K
Q7
Q6
MEG Ω
V REF
R39 6.99M
R40 25K
R41 777.15K
1000K Ω
R42 1K
R43 70.555K
100K Ω
R44 100
R45 330K
R58 243K
1KΩ
R46 100K
R47 7.0223
CR7
CR8
CR9
CR10
CURRENT LADDER
MULTIVIBRATOR
CR11
Q8
R51 390
CR12
Q9
CR18
CR13
K7
CR14
K6
CR15
K4
CR16
K5
CR19
K2
CR20
K1
CR22
K8
R48 3.9K
R49 3.9K
R50 3.9K
R52 3.9K
R53 3.9K
R55 22K
A3
RELAY DRIVERS
-18V INPUT FROM POWER SUPPLY
18
+18V INPUT FROM POWER SUPPLY
16
REFERENCE VOLTAGE FROM LADDER SEE A/D SCHEMATIC
12
11 LOGIC COMMON
15 SIGNAL COMMON
5 KΩ CONTROL LINE
14 MV CONTROL LINE
1 RANGE b¹ CONTROL
4 KΩ CONTROL LINE
2 RANGE a¹ CONTROL
13 MV CONTROL LINE
6 K8 CONTROL LINE
9 MΩ CONTROL LINE
10 MΩ CONTROL LINE
Q10
CR21
CR23
CR24
R54 3.9K
CR25
K3
TP5
FUNCTIONAL SCHEMATIC DIAGRAM
MODEL 8300A
MILLIVOLTS/OHMS CONVERTER
SCHEMATIC NO 7
SER NO 123 & ON
REV a
FLUKE JOHN FLUKE MFG. CO., INC.
P.O Box 7428 Seattle, Washington 98133


GUARD BOUNDARY
INSIDE GUARD
OUTSIDE GUARD
EXT. REF. CONT. LINE
FILTER CONT. LINE
RANGE
RANGE
POLARITY SIGNAL SEE LOGIC SCHEM.
KΩ CONT. LINE
MΩ CONT. LINE
MV CONT. LINE
VAC CONT. LINE
VDC CONT. LINE
CCO SEE LOGIC SCHEMATIC
ZERO
TRIG
+5V INSIDE GUARD
LOGIC GND
+5VDC
SHIFT REGISTER MEMORY
DIGITS COUNTER
STEERING FLIP-FLOP
OVERLOAD SIGNAL
TO CR1 CATHODE
J1 (CONNECTOR "A")
J2 (CONNECTOR "B")
Z IN
Y IN
X IN
W IN
Z OUT
Y OUT
X OUT
W OUT



FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
EXTERNAL REFERENCE UNIT

SCHEMATIC NO. 10

SER. NO. 123 & ON	REV.
	a

FLUKE JOHN FLUKE MFG. CO., INC.
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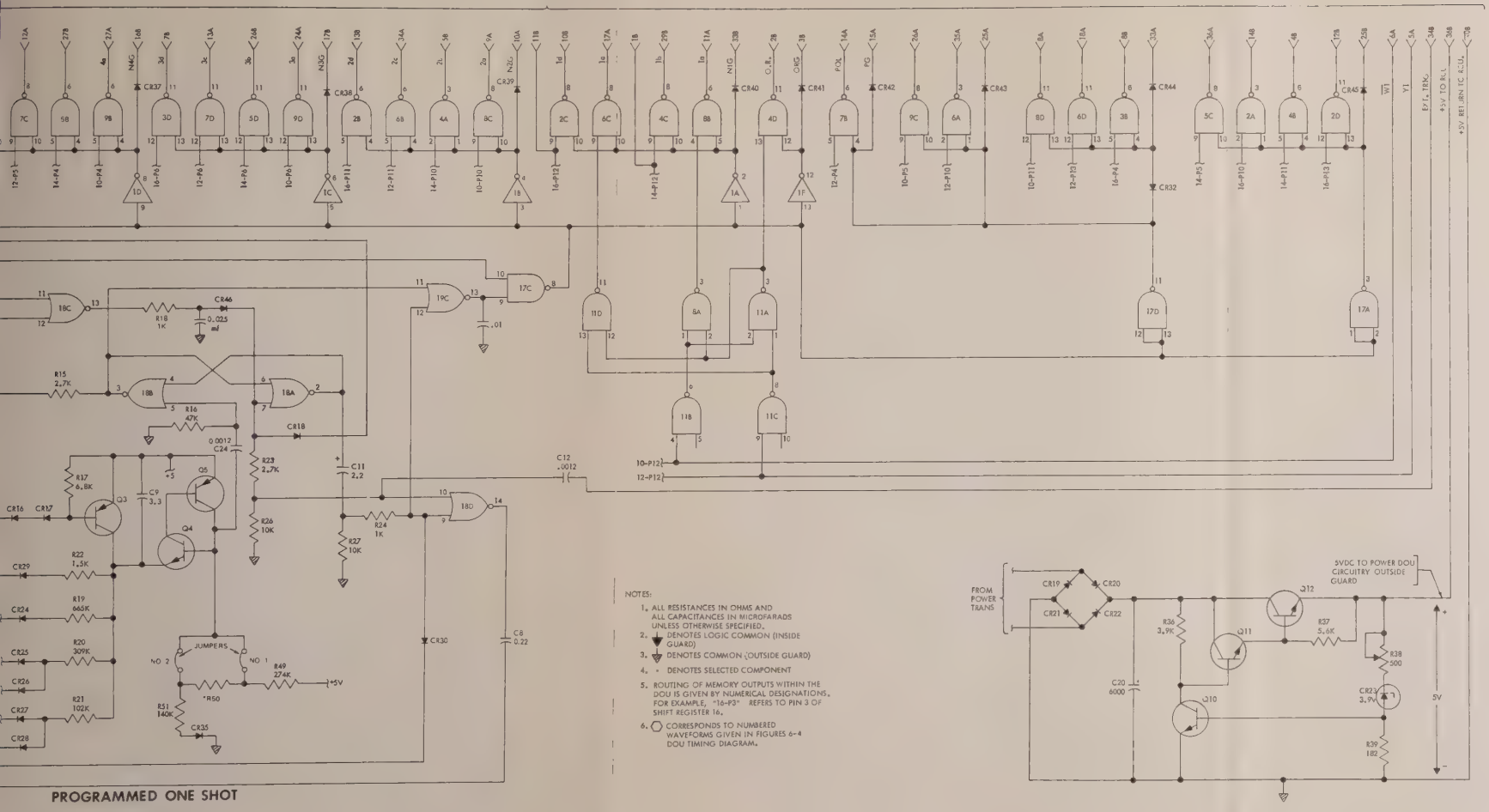
DOU REAR PANEL CONNECTORS



PROGRAMMED ONE SHOT

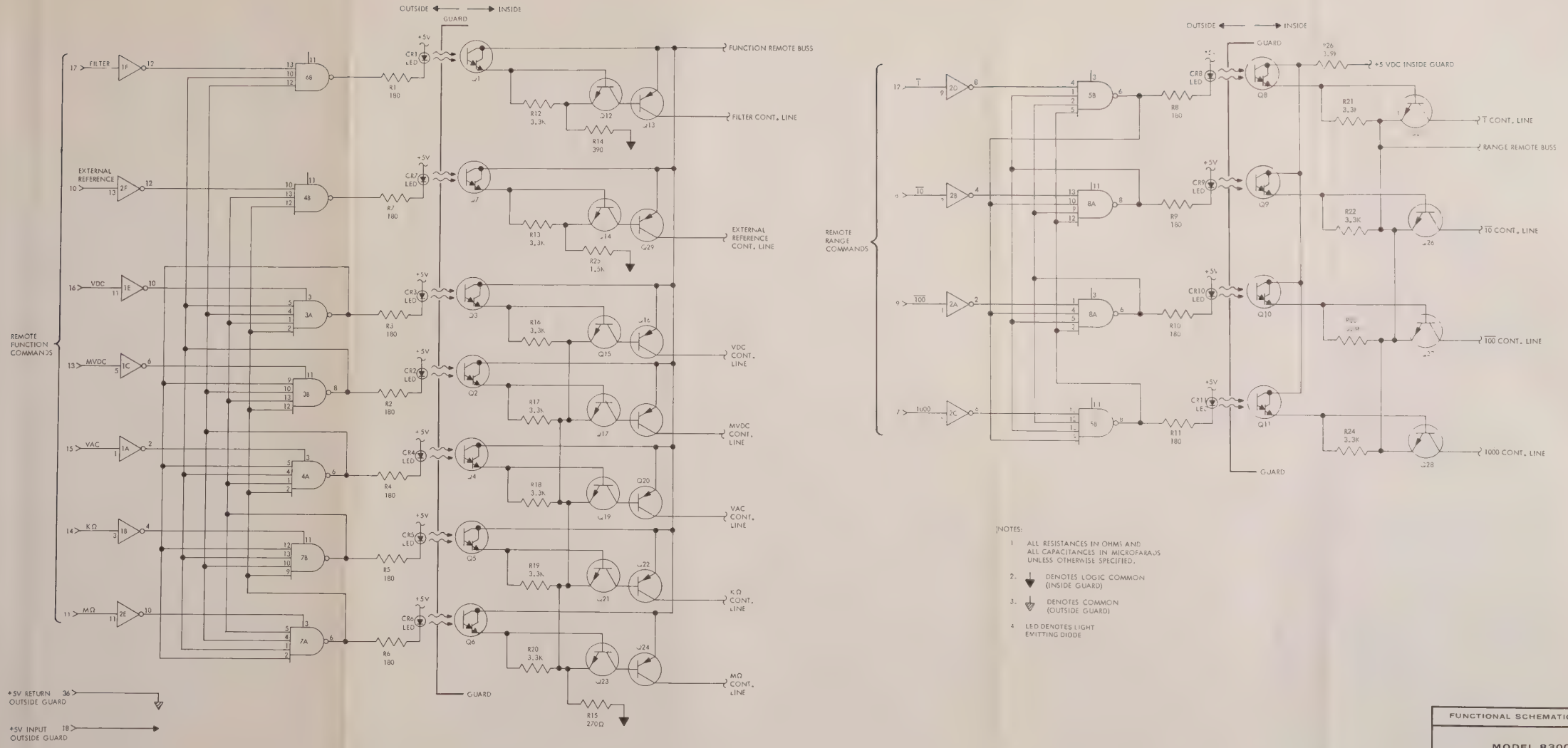
NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ▽ DENOTES COMMON (OUTSIDE GUARD)
4. ▪ DENOTES SELECTED COMPONENT
5. ROUTING OF MEMORY OUTPUTS WITHIN THE DOU IS GIVEN BY NUMERICAL DESIGNATIONS. FOR EXAMPLE, "16-P3" REFERS TO PIN 3 OF SHIFT REGISTER 16.
6. ◯ CORRESPONDS TO NUMBERED WAVEFORMS GIVEN IN FIGURES 6-4 DOU TIMING DIAGRAM.

FROM POWER TRANS

5VDC TO POWER DOU CIRCUITRY OUTSIDE GUARD

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DATA OUTPUT UNIT	
SCHEMATIC NO. 8	
SER NO 193 & ON	REV a
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle Washington 98133	

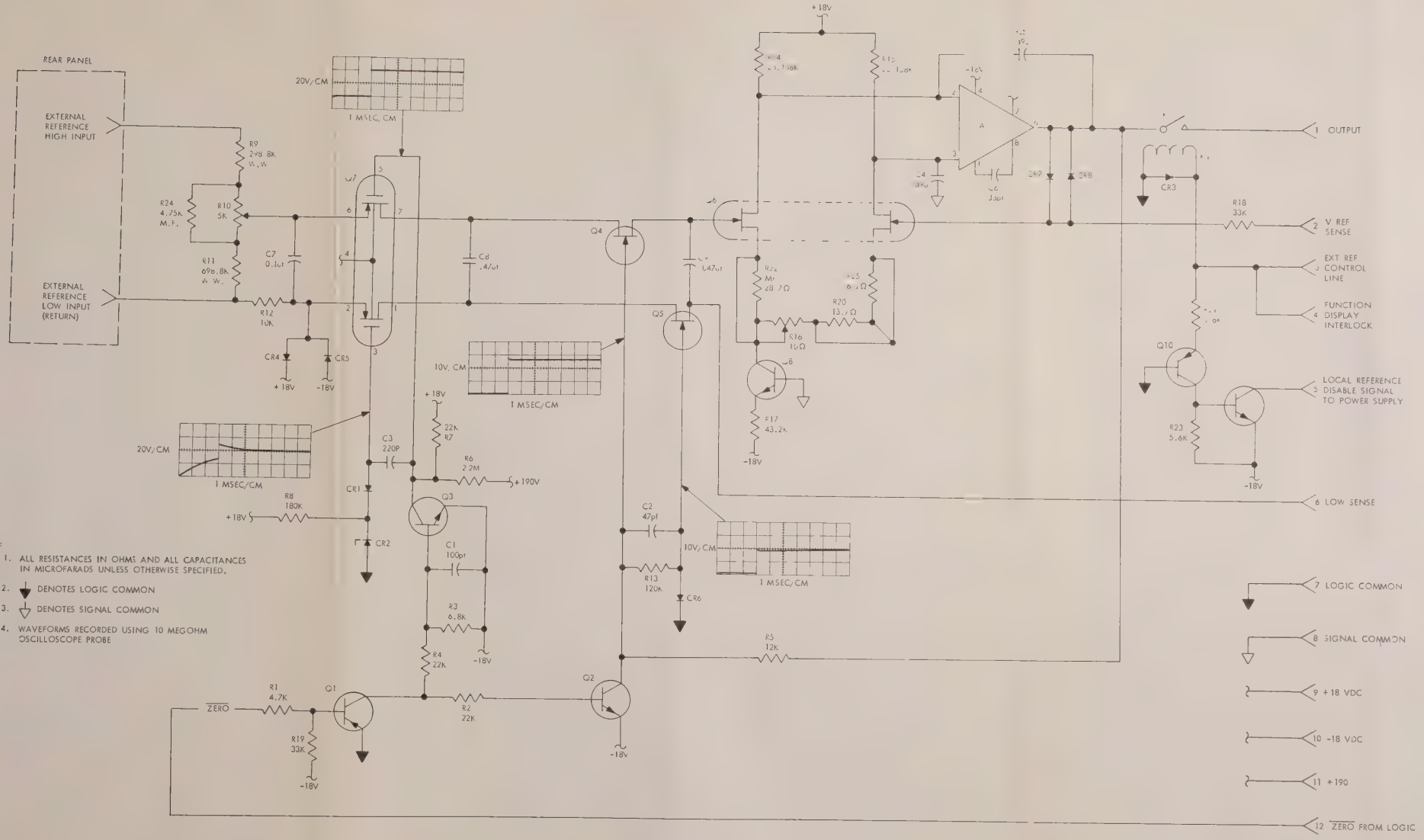


NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ⏚ DENOTES COMMON (OUTSIDE GUARD)
4. LED DENOTES LIGHT EMITTING DIODE

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A REMOTE CONTROL UNIT	
SCHEMATIC NO 9	
SER NO 123 & ON	REV. 2

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ▽ DENOTES SIGNAL COMMON
4. WAVEFORMS RECORDED USING 10 MEGOHM OSCILLOSCOPE PROBE

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A EXTERNAL REFERENCE UNIT	
SCHEMATIC NO. 10	
SER NO. 123 & ON	REV a
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

ERRATA

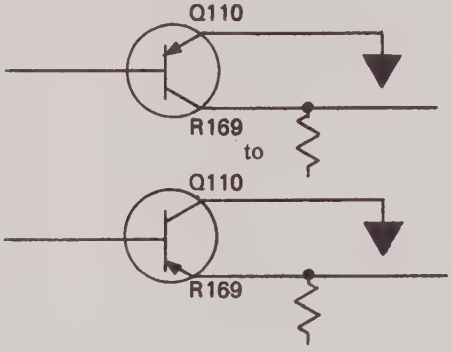
FLUKE MODEL 8300A SCHEMATICS

Schematic No. 1, Buffer

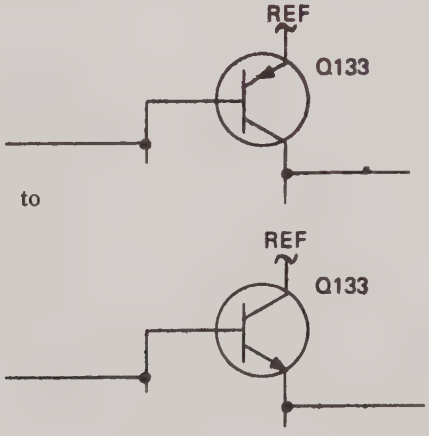
1. Change reference designation Q17 to Q12.

Schematic No. 2, A/D Converter

1. R162 should be 100k.
2. R119 should be 5.6k.
3. Change Q110 circuit from



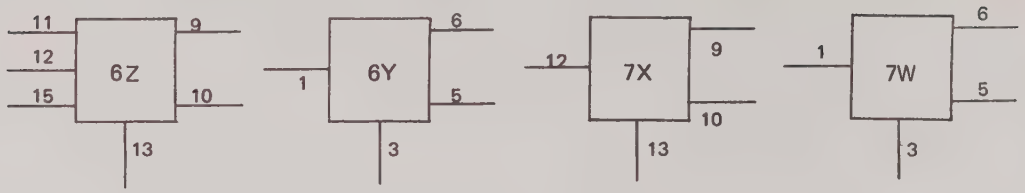
4. R153 should be 32.4k.
5. Change reference designation Q135 to Q155.
6. Change Q133 circuit from



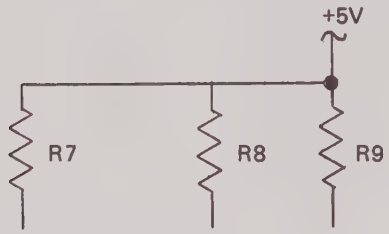
Schematic No. 3, DVM Logic and Control

1. Add reference designation and value to resistor located between test point TP5 and capacitor C5:

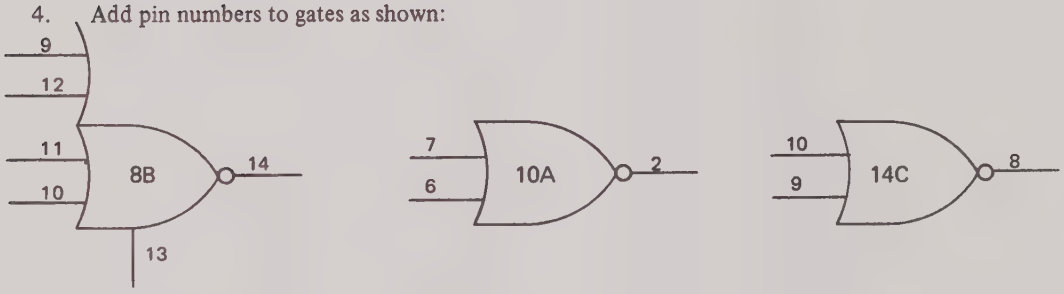
2. Add pin numbers to binary counter flip flops as shown:



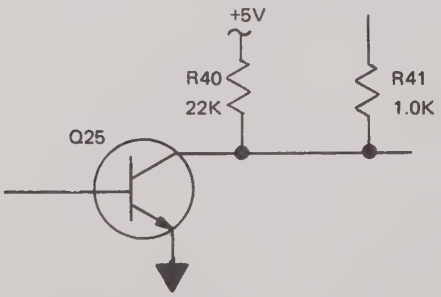
3. Add +5 volt line to junction of R7, R8, and R9:



4. Add pin numbers to gates as shown:



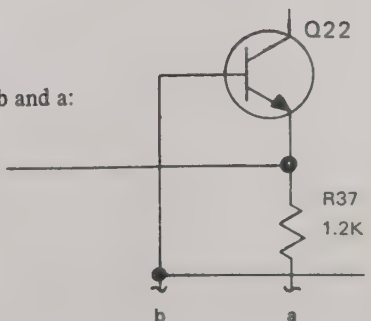
5. R51 should be 2.7k.
6. Add +5 volts through resistor to Q25 collector:



7. R25 should be 22k.

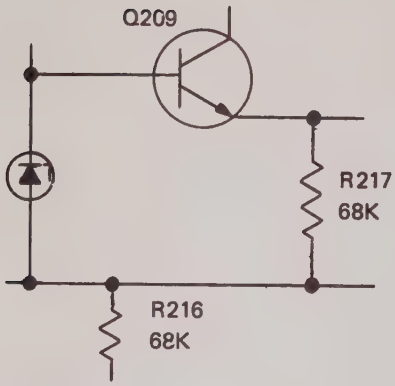
Schematic No. 4, Display

1. Change designations of input signals to Q22 from $\overline{b}$ and $\overline{a}$ to b and a:

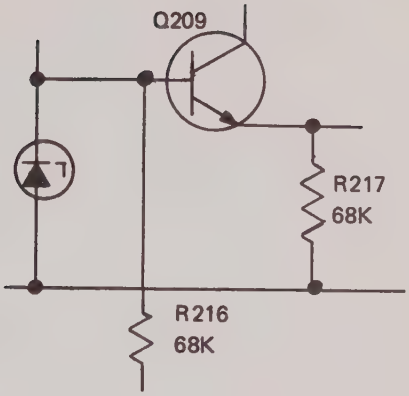


Schematic No. 5, Power Supply

1. Change circuitry from:



to:

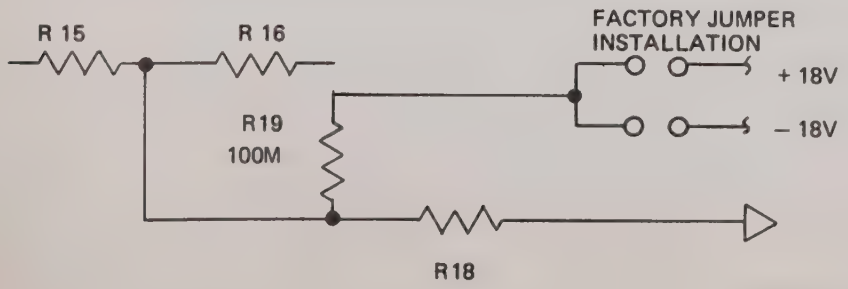


Schematic No. 6, AC Converter

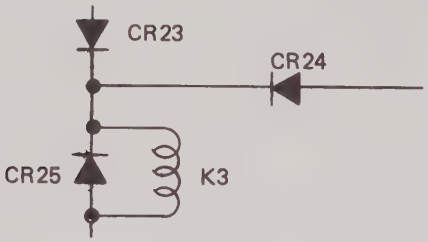
1. C4 should be 0.8 – 10 pf.
2. C6 should be 9 – 35 pf.
3. R7 should be 15Ω.
4. C26 should be 390 pf.

Schematic No. 7, Millivolt/Ohms Converter

1. R3 should be 220k.
2. C2 should be 0.1 uf.
3. Change R62 51Ω to R60 22Ω.
4. Change R61 5.1Ω to R59 4.7Ω.
5. C13 should be 0.1 uf.
6. Change R60 510Ω to R61 240Ω.
7. R33 should be 715k.
8. R36 should be 715k.
9. C15 should be 5600 pf.
10. C14 should be 4700 pf.
11. C11 should be 2.2 uf.
12. Add the following circuitry at the junction of R18 and R16, as shown:

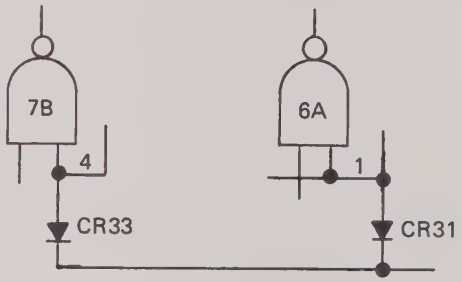


13. Change reference designation of CR12 to CR17.
14. Change circuitry of CR23 as shown:



Schematic No. 8, Data Output Unit

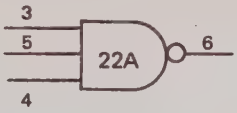
1. C15 should be 0.68 uf.
2. R21 should be 100k.
3. Reference designation of .01 uf capacitor at pin 9 of gate 17C is C10.
4. Add diodes CR31 and CR33 as shown:

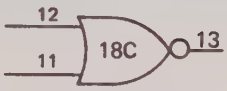


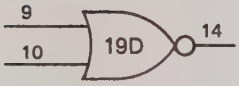
5. Correct/add signal designations for connector pins as shown in following table:

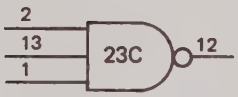
Pin/Connector	Signal Designation
15B	N5G
6B	4d
12A	4c
27B	4b
11B	$\overline{Z1}$
1B	$\overline{X1}$
26A	a
35A	b
8A	FILTER
18A	EXT REF
8B	DC
33A	FIG
36A	AC
14B	MV
4B	MΩ
12B	KΩ
25B	F2G

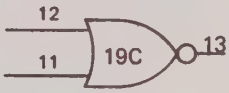
6. Connector pin designation of "+5V RETURN TO RCU" should be 30B.
7. Add/correct pin numbers of components as shown:

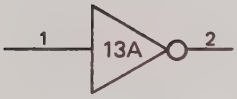


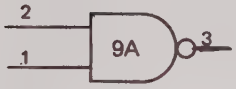






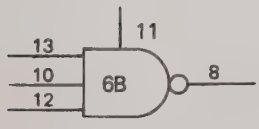


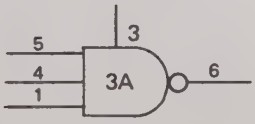


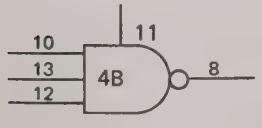


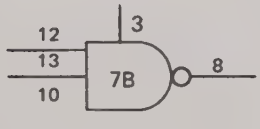
Schematic No. 9, Remote Control Unit

1. R14 should be 270Ω.
2. R25 should be 820Ω.
3. R15 should be 180Ω.
4. Add missing transistor reference designation, Q18.
5. Add output pin numbers to NAND gates as shown:









1970 PRODUCT DIRECTORY

JOHN FLUKE MFG. CO., INC.

FLUKE®

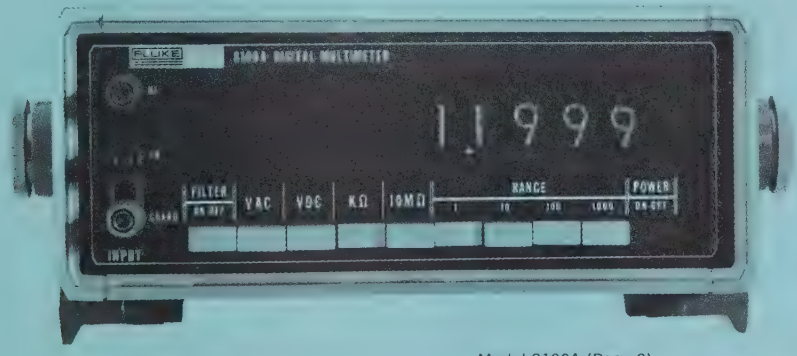
NEW-NEW-NEW

A New Approach to Digital Voltmeters

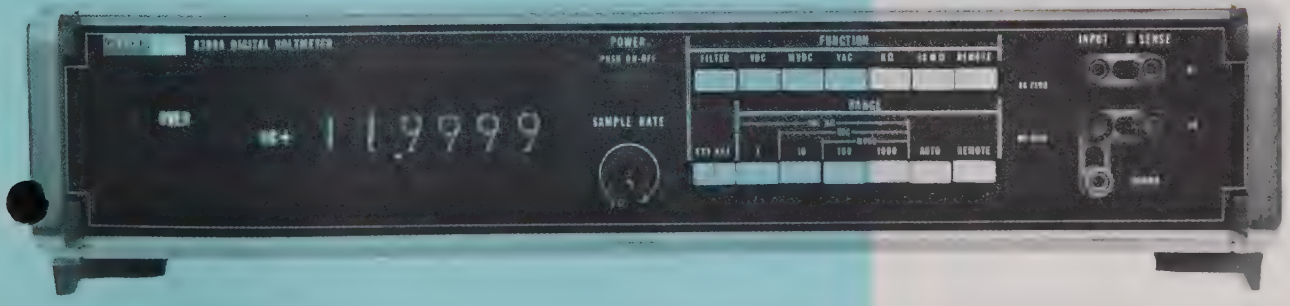
The new Fluke family of digital voltmeters uses circuit disciplines never before adapted to this kind of instrumentation. The Models 8100A and 8300A offer an analog to digital conversion technique based on storage capacitors, a single BCD counter and a resistive ladder network to serially determine and display all digits. The technique is called Recirculating Remainder A to D conversion.

The Model 8100A Digital Multimeter features four full digits plus "1" for 20% overranging; rechargeable battery operation; push-button selectable functions; four range measurement for AC and DC to 1200 volts and five range measurement in ohms.

The Model 8300A Digital Voltmeter features five full digits plus "1" for 20% overranging; auto ranging; 25 millisecond sampling speed; full systems capability with timing signals and ready indicator, low cost options including AC voltage, millivolt/ohms, isolated external reference (4 terminal ratio) fully isolated remote programming and data output, and AC/AC ratio.



Model 8100A (Page 2)



Model 8300A (Page 3)

Table of Contents

Calibrators
- DC Voltage 5
- Meter 8
- Programmable Voltage/Current 4
- Voltage/Current 8

Calibration Systems 9

Electronic Galvanometers 10

Frequency Comparators 11

Frequency Distribution Amplifier 11

Frequency Synthesizers 10, 11

Multimeters
- Differential 7
- Digital 2

Null Detector Microvoltmeter 8

Omega Commutator 11

Power Supplies
- High Voltage 9
- Nims High Voltage 5

Rack Mounting Configurations 6

Ratio Measurement Devices 9

Thermal Transfer Standard 7

Transit Cases 7

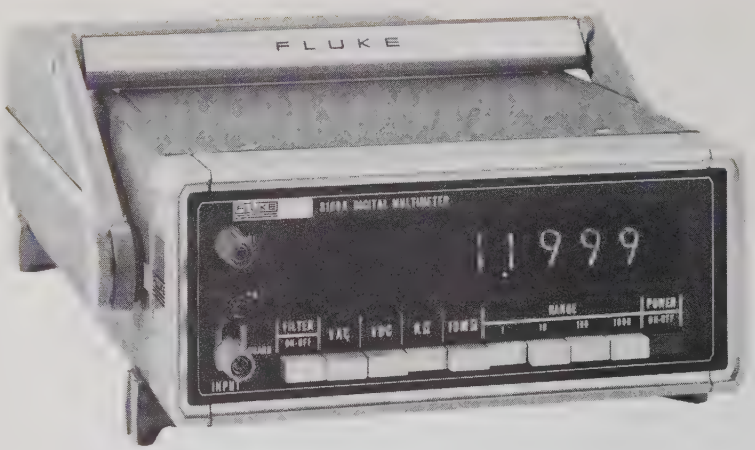
VAW Meter 12

VLF Receiver/Comparator 11

Voltage Dividers 7

Voltmeters
- Differential 6
- Digital 3
- RMS Differential 7
- RMS Digital 7

DIGITAL MULTIMETER-MODEL 8100A



MODEL 8100A 0.02% DIGITAL MULTIMETER HAS COMPLETE PORTABILITY

- Measures AC and DC volts in four ranges to 1200 volts
- Measures ohms in five ranges to twelve megohms
- Optional rechargeable battery pack operation
- Automatic polarity indication
- All functions are push-button selectable
- Active 2-pole switchable filter
- Four full digits plus "1" for 20% overranging
- Meets specifications for 90 days from 15°C to 35°C, and 0 to 80% relative humidity
- New conversion method reduces power consumption.

SPECIFICATIONS

GENERAL

Size:	3½" high x 8½" wide x 15" deep
Power:	115/230 VAC±10%, 50 to 500 Hz. 10 watts 8 hours operation on optional batteries
Weight:	10.5 lbs. with batteries
Price:	Full multimeter, $695
Option	01—rechargeable battery power, $100
Accessories:	■ HF probe ■ HV probes ■ Switched AC-DC current shunts ■ Ruggedized case ■ Rack mounting brackets

DC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy:	±(0.05% of reading + 0.01% of range)
30 Days:	±(0.02% of reading + 0.01% of range) 20°C to 30°C
Input Impedance:	10 megohms all ranges at all times
Speed:	0.5 sec without filter 1.0 sec with filter
Common Mode Rejection Ratio:	> 100 db DC to 60 Hz with filter (Infinite when battery operated.)
Normal Mode Rejection Ratio:	50 db at 60 Hz with filter

AC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy:	±(0.2% reading + 0.05% of range) 50 Hz to 10 KHz ±(0.5% reading + 0.05% of range) 30 Hz to 50Hz, 10 KHz to 20 KHz
Speed:	< 3.0 sec
Input Impedance:	1 megohm paralleled with < 30 pf.

OHMS

Ranges:	1K, 10K, 100K, 1M, 10M
Accuracy:	±(0.1% reading + 0.01% of range)
Speed:	0.5 secs thru 1 megohm without filter 3.0 secs 10 megohm without filter
Voltage Across Unknown R:	1V at full scale decreasing linearly to 0 volts.

DIGITAL VOLTMETER-MODEL 8300A

Model 8300A 0.005% DIGITAL VOLTMETER HAS TOTAL BUILT-IN SYSTEMS CAPABILITY

- Basic unit measures 0 to 1100 volts DC in three ranges
- New conversion method for increased reliability
- Reads out in five full digits plus "1" for 20% overranging
- 25 millisecond sampling speed
- Automatic ranging and polarity
- Fully guarded with 140 db common mode rejection
- Active 3 pole switchable filter with 60 Hz notch
- Normal Mode Rejection Ratio 60 db, 50 Hz and up
- Full systems capability with timing signals, ready indicators and flags
- DTL-TTL compatible Data Output and Programming
- Meets all 90 day specifications from 20°C to 30°C, and 0 to 70% RH.

WITH LOW COST OPTIONS, TAILOR THE FLUKE 8300A DVM TO YOUR EXACT SYSTEM REQUIREMENT.

- AC voltage measurement in four ranges 0 to 1100 volts
- Millivolt/Ohms option on one board
- External Reference for bipolar ratio measurement
- Fully isolated remote programming
- Fully isolated data (printer/computer) output
- AC/AC ratio
- Add options any time on order or in the field for the same cost

SPECIFICATIONS

Ranges:	10V, 100V, 1000V
Accuracy:	±(0.005% of reading + 0.001% of range) 24 hours; 23°C ±1°C ±(0.01% of reading + 0.003% of range) 90 days
Input Impedance:	> 10^{10} ohms at all times on 10V range 10^{7} ohms on 100V and 1000V ranges
Normal Mode Rejection Ratio:	> 60 db, 50 Hz and up
Common Mode Rejection Ratio:	140 db DC to 60 Hz (filtered) with 1K unbalance to low terminal
Speed:	25 ms max unfiltered 500 ms max unfiltered
Max Auto Range:	80 ms unfiltered

GENERAL

Variable Sample Rate:	Local: Variable 10/sec to 1 per 3 sec External: 40/sec maximum
Maximum Conversion Time:	25 ms, after sample pulse
Warmup:	30 minutes
Operating Temperature:	0°C to 50°C
Power:	115/230 VAC±10% at 50 to 440 Hz 20 watts with all options
Size:	3½" high x 17½" wide x 15" deep
Weight:	12 to 15 lbs.
Price (8300A):	$1295

OPTIONS—Refer to page 4

8300A OPTIONS

AC VOLTS

Ranges:	1V, 10V, 100V, 1000V
Accuracy: (90 days)	±(0.1% of reading + 0.005% of range) 50 Hz to 20 kHz. Total freq. response, 30 Hz to 100 kHz
Input Impedance:	1 megohm < 100 pf
Speed:	500 ms to within 0.1% of final reading
Price: (—01 option)	$450.00

EXTERNAL REFERENCE (RATIO)

Reference Range	+2V to +10.5V
Accuracy:	$\pm(0.01\% \text{ of reading} + \frac{0.003\% \times 10V}{V_{ref}} \text{ of range})$
Input Resistance:	1 megohm
Speed:	500 ms to ±0.01% of final reading
Isolation:	True 4-terminal ratio capability. Up to ±12V commons separation
Normal Mode Rejection Ratio:	> 30 db at 60 Hz.
Price: (—05 option)	$200.00 (requires —07 rear term. acc. $25.00)

DATA OUTPUT (Fully Isolated)

Data Available:	Function, Range, Polarity and Digits.
Flags:	Ready, Overload.
Controls:	External Trigger, Fast/Normal Data Transfer
Logic Levels	+5V thru 6K=1, 0V=0 (Series 930 DTL)
Price: (—03 option)	$500.00

REMOTE CONTROL (Fully Isolated)

Input Definition:	Series 930 DTL
Control Modes:	DTL, TTL or contact closure
Logic Levels:	+5V; no command 0V or switch closure; call up function
Price: (—04 option)	$200.00

* MV/Ohms and AC/AC ratio options cannot simultaneously be installed in an 8300A. The 8300A will accept either option at any time, however.

MILLIVOLT/OHMS*

Resistance Ranges:	1K, 10K, 100K, 1000K, 10M
Accuracy: (90 days)	1K thru 100K: ±(0.01% of reading + 0.003% of range) 1000K: ±(0.02% of reading + 0.003% of range) 10M: ±(0.05% of reading + 0.003% of range)
Measurement Voltage:	1.1V for 1K and 10K at full range 10V for 100K to 10M at full range 0 at short circuit input
Speed:	Within 0.01% of final reading in 75 ms 100K thru 10M and 1 sec 1 K and 10K
Millivolt Ranges:	100 mv, 1000 mv
Accuracy: (90 days)	100 mv: ±(0.01% reading + 0.01% full scale) 1000 mv: ±(0.01% reading + 0.003% full scale)
Input Impedance:	1000 mv: = 1000 MΩ, 100 MV = 100 MΩ
Speed:	100 mv: 3 sec to within 0.01% of final reading 1000 mv: 1 sec to within 0.01% of final reading
Normal Mode Rejection Ratio:	>60 db, 50 Hz and up
Common Mode Rejection Ratio:	>140 db DC to 60 Hz
Overload:	1100V DC without damage
Price: (—02 option)	$350.00

AC/AC RATIO *

Reference Voltage Range:	0.2V to 105V in three ranges.
Input Impedance:	1 megohm shunted by < 100 pf
Ratio Accuracy:	$\pm(0.05\% \text{ of input} \frac{+0.005\% \times \text{Ratio Range}}{E_{Ref}}$ % of range) 50 Hz –20 kHz.
Price: (—08 option)	$700 (Note: Options —01, —05, and —07 must be installed to use AC/AC Ratio option)

NEW-NEW-NEW

PROGRAMMABLE VOLTAGE/ CURRENT CALIBRATOR– MODEL 3330A

The Model 3330A is a fully programmable constant voltage/constant current Calibrator. This Calibrator provides output voltages from 0-1000V in 3 ranges and constant current outputs from 0-100 ma in three ranges, with 11% overranging on each range. Voltage accuracy is ±0.005%. Constant current accuracy is ±0.01%.

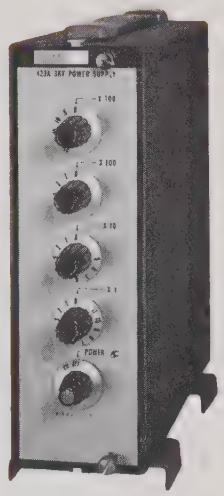
BRIEF SPECIFICATIONS

MODE	VOLTAGE RANGE	MAX. CURRENT	CURRENT RANGE	COMPLIANCE VOLTAGE	ACCURACY	REGULATION LINE-LOAD	STABILITY PPM OF OUTPUT	PRICE
CONSTANT VOLTAGE	10, 100, 1000V	100 ma 50 ma			±0.005%	5 ppm of output	25 ppm Per mo.	$2995.00
CONSTANT CURRENT			1, 10, 100 ma	1000V 500V	±0.01%	5 ppm of range	50 ppm Per mo.	

NEW-NEW-NEW

NIMS HIGH VOLTAGE POWER SUPPLY-MODEL 423A

Designed for Nuclear Instrument Module Systems (NIMS), The Model 423A is a versatile high voltage power source in a small package. Contained in either a portable bench case or a NIMS bin, the Model 423A features remote analog slewing of the output, or manual operation in steps of 10, 100 and 500 volts. A Sweep Vernier allows control of the output from zero to the calibrated dial settings.



BRIEF SPECIFICATIONS

OUTPUT VOLTAGE	OUTPUT CURRENT	ACCURACY	RESOLUTION	SLEWING	RIPPLE & NOISE	OVERLOAD PROTECTION	POLARITY
0 to ± 3000 VDC	0-10 ma	0.25% or 1.25V whichever is greater	100 mv	0 to dial setting with vernier	5 mv p-p	Output limited to 15 ma	Reversible at rear panel

SIZE 3 inches by 9 inches by 10 inches

VOLTAGE CALIBRATION

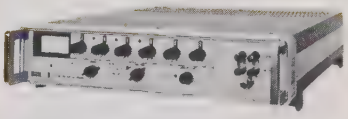
0 to 2500 V in 5 steps of 500V
0 to 400V in 4 steps of 100V
0 to 90V in 9 steps of 10V
0 to 10V vernier

PRICE		
	Basic Unit	$460.00
	Carrying Case	$35.00
	△ E Option	$50.00

NEW-NEW-NEW

DC VOLTAGE CALIBRATOR– MODELS 341A AND 343A

The Fluke Models 341A and 343A DC Voltage Calibrator are outstanding new additions to the Fluke line of all solid-state ultra-precise and stable DC Calibrators. Both instruments cover 0-1111 volts dc in three ranges of 10, 100, and 1000 volts, each with 11% overranging. For the Model 341A, calibration accuracy is an absolute ±0.01% of setting from 0.3 volt to 1111 volts. Calibration accuracy for the Model 343A is ±0.003% of setting from 0.7 volt to 1111 volts. Each Model has current limiting crowbar protection and a four-terminal floating output.



Model 341A

Model 343A

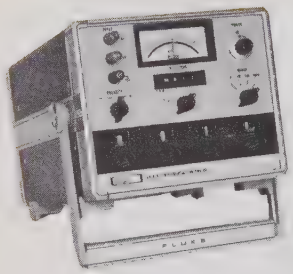
BRIEF SPECIFICATIONS

MODEL	OUTPUT VOLTAGE	CURRENT OUTPUT	ACCURACY	REGULATION LINE-LOAD	STABILITY % PER MO.	RIPPLE (rms)	RESOLUTION PPM OF RANGE	PRICE
341A	0 to 1111.110V	25 ma	±0.01% (6 mos.)	0.0005%	±0.003%	<100 uv	1 ppm	$1195.00
343A	0 to 1111.1110V	25 ma	±0.003%	0.0005%	±0.0015%	<50 uv	0.1 ppm	$1795.00

VOLTMETERS

Fluke AC/DC and DC Differential Voltmeters offer the widest range of performance and accuracy in the market. Most units operate from either internal rechargeable batteries or 115/230V, 50-440 Hz line power. Battery power is essential for measurement where maximum accuracy demands complete line isolation. Input ranges are 1, 10, 100 and 1000V each with 10% overranging. Fluke Differential Voltmeters are electrically and mechanically designed to perform under the extremes of temperature, shock, vibration and humidity. The internal reference voltage is developed from matched zener diodes that are selected to establish excellent stability, tracking and temperature coefficient parameters. Fluke manufactures all of the precision wire-wound resistors used in these instruments. The all solid-state differential voltmeters are lightweight for portability and are provided with a tilt-back bail, or functional detented handle for operator convenience. Recorder output feature is available on all Fluke Differential Voltmeters.

DIFFERENTIAL VOLTMETERS



Model 891A

Model 883A

Model 881A

Solid State DC

MODEL	INPUT	DIFF. ACCURACY % OF INPUT	POWER	PRICE
881A	0-1100 VDC	±0.005%	115 or 230 VAC	881A – $895.00 881AB – $995.00
885A	0-1100 VDC	±0.0025%	115 or 230 VAC	885A – $1060.00 885AB – $1160.00
891A & AR	0-1100 VDC	±0.01%	115 or 230 VAC	891A & AR – $745.00 891A-01 – $845.00
895A	0-1100 VDC	±0.0025%	115 or 230 VAC	895A – $1250.00
896A	0-15 kv	±0.005% ±0.1% from 1 kv to 15 kv	115 or 230 VAC	896A – $1995.00

Solid State AC/DC

MODEL	INPUT	DC ACCURACY % OF INPUT	AC ACCURACY %	FREQUENCY RANGE	POWER	PRICE
883A	0-1100V	±0.005%	±0.1%	20 Hz to 5 kHz from 1 mv to 1100V	115 or 230 VAC	883A – $1295.00 883AB – $1395.00
887A	0-1100V	±0.0025%	±0.1%	20 Hz to 5 kHz from 1 mv to 1100V	115 or 230 VAC	887A – $1495.00 887AB – $1595.00
893A & AR	0-1100V	±0.01%	±0.15%	20 Hz to 20 kHz from 1 mv to 1100V	115 or 230 VAC	893A & AR – $1045.00 893A-01 – $1145.00

RACK MOUNTING CONFIGURATIONS

Kits are available for side-by-side, center or left/right side rack mounting of most half rack width Fluke Voltmeters. Kits are also available for mounting full rack width voltmeters and calibrators.

TRUE RMS DIGITAL VOLTMETER–MODEL 9500A

The 9500A precisely measures the true RMS value of any AC signal up to 1100 volts RMS regardless of waveshape or harmonic content. Input range selection, decimal point, and calibration are truly automatic. Nixie® tubes provide a digital display, readable over a wide viewing angle. Both display and range may be varied by means of front panel control.

VOLTAGE RANGE: 1 mv to 1100V RMS

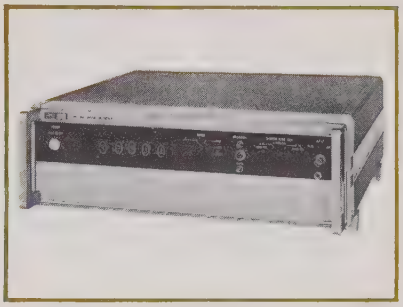
ACCURACY: ±(0.05% of input + 0.015% of range) from 50 Hz to 10 kHz
Reduced accuracy specifications from 20 Hz to 700 kHz

FREQUENCY: 20 Hz to 700 kHz

INPUT RESISTANCE: 1 megohm shunted by 17 pf

INPUT POWER: 115/230 VAC, 50-440 Hz

PRICE: $2485.00



TRUE RMS DIFFERENTIAL VOLTMETER–MODEL 931B

The Model 931B combines the advantages of a true RMS voltmeter for accurate measurement without waveform error and the null balance accuracy of a differential voltmeter.

VOLTAGE RANGE:
Differential Mode: 0.01 to 1100V RMS in 5 ranges (10% overranging)
Direct Mode: 0.003 to 1100V RMS in 11 ranges

CREST FACTOR: Differential Mode: 10

INPUT POWER: 115/230V AC, 50 – 440 Hz

ACCURACY:
Differential Mode: ±(0.05% of reading + 0.005% of range) from 30 Hz to 50 kHz. Reduced accuracy specifications from 2 Hz to 1 MHz
Direct Mode: ±3% of end scale

INPUT IMPEDANCE: 1 megohm shunted by less than 8 pf

PRICES: $995.00

PRECISION VOLTAGE DIVIDERS–MODELS 80D AND 80E

The Models 80D and 80E are tapped for 10 and 1V outputs at rated input, for use with all Fluke differential voltmeters and any conventional potentiometer.

MODEL NO.	MAX. INPUT VOLTAGE	TOTAL RESISTANCE	DIVISION RATIO 500V OUT	DIVISION RATIO 10V OUT	DIVISION RATIO 1V OUT	DIVISION RATIO ACCURACY	PRICE
80E-5	5 kv	5 Meg	–	500:1	5,000:1	±0.01%	$ 350.00
80E-10	10 kv	10 Meg	–	1000:1	10,000:1	±0.01%	$ 395.00
80D-30	30 kv*	30 Meg	60:1	3000:1	30,000:1	±0.01%	$1,195.00

*Intermediate voltages between 10 KV and 30 KV available upon request.

DIFFERENTIAL MULTIMETER-MODEL 853A

The Model 853A is an all solid-state, extremely accurate low cost multimeter utilizing differential techniques to measure AC/DC voltages and current and resistance. The instrument may be operated from line and/or rechargeable or replaceable batteries.

ACCURACY: ±(0.2% + 0.02% FS) for DC voltage and current
±(0.5% + 0.05% FS) for AC voltage and current

VOLTAGE RANGE: 0 – 1100 VAC/DC in 4 ranges

FREQUENCY RANGE: 20 Hz to 30 kHz

CURRENT RANGE: 0 – 10 amps AC/DC in 6 ranges

RESISTANCE RANGE: 0 – 100 megohms in 7 ranges

ACCURACY: ±(0.2% + 0.01% FS)

OVERLOAD PROTECTION: 1200V RMS or DC on any range. 12 amps on 10 amp range. 2 amps on all other ranges

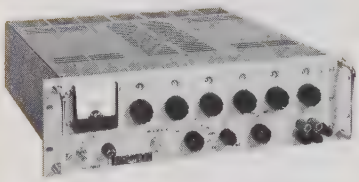
PRICE: $545.00 Replaceable Battery
$595.00 Rechargeable Battery

TRANSIT CASES

Where operation and storage in severe relative humidity conditions (up to and including 100%) are required, most Differentials are available with splash-proof panel and MIL-T-945A combination case.

VOLTAGE AND CURRENT CALIBRATORS

Model 335A



Model 382A

The Fluke line of voltage and current calibrators combine ruggedness and reliability with extreme accuracy, and stability. Most units are provided with current and voltage limit functions. All solid-state models are equipped with zener diode reference elements, housed in proportionately controlled temperature ovens.

MODEL	VOLTAGE	CURRENT	REGULATION LINE	REGULATION LOAD	STABILITY, % HOUR	STABILITY, % DAY	STABILITY, % PER MO.	CALIBRATION ACCURACY	MAX. RIPPLE RMS	PRICE
313A	0-50	0-2A	0.0005	0.0005	0.002	0.0025	0.005	0.01%	50 uv	$1395.00
332B	0-1111	0-50 ma	0.0002	0.0002	0.002 /year			0.002%	20-40 uv	$2445.00
335A*	0-1111	0-50 ma	0.0002	0.0002	0.002 /year			0.002%	20-40 uv	$2645.00
	(Model 335A is also a 20 ppm differential voltmeter and nine range, high input impedence galvanometer)									
382A**	0-50	0-2A	0.0005	0.0005	0.002	0.0025	0.005	0.01%	50 uv	$1595.00
382A†	0-50	0-2A (4 ranges)	0.0005	0.001	0.0025		0.005	0.02%	0.002% of range	

*Calibrator Portion Only.
**Voltage Mode.
†Current Mode.

METER CALIBRATOR–MODEL 760A

The Model 760A Meter Calibrator is a complete all solid-state calibration system for AC and DC voltmeters, ammeters, ohmeters, and multimeters. Interlocks and safety features are provided to protect both the operator and the instrument being calibrated.

	DC VOLTAGE AND CURRENT	AC VOLTAGE AND CURRENT
VOLTAGE RANGE:	0.001V to 1000V in 0.1 mv steps	0.001V to 1000V in 0.1 mv steps
VOLTAGE ACCURACY:	±(0.1% of setting + 25 uv) Also ±0.33% at 1 mv, 3 mv, and 10 mv	±(0.25% of setting + 25 uv) Also ±0.33% at 1 mv, 3 mv, and 10 mv
CURRENT RANGE:	1 ua to 10A in 1 ua steps	1 ua to 10A in 1 ua steps
CURRENT ACCURACY:	±(0.25% of setting + 0.025 ua)	±(0.25% of setting +0.025 ua)
FREQUENCY:		60 Hz and 400 Hz (60 Hz phase locked to power line)
RESISTANCE:		
Range:	0 to 10 megohms	
Accuracy:	±(0.1% of setting + 0.5 ohm)	
Resolution:	1 ohm	
PRICE:	$2845.00	

NULL DETECTOR MICROVOLTMETER–MODEL 845AB

The Models 845AB and 845AR are designed for extremely high input resistance, sensitivity and isolation. Typical applications are standardization of voltage dividers and true comparison of standard cells, ratio measurements and many more.

INPUT RANGES: 1 uv to 1000 VDC in 19 end-scale ranges

ACCURACY: ±(2% end scale + 0.1 uv)

INPUT RESISTANCE: 100 megohms on 300 mv range and above
10 megohms on 100 mv range and below

INPUT POWER: 845AB rechargeable battery or 115/230 VAC ±10%, 50-440 Hz
845AR 115/230 VAC ±10%, 50-440 Hz

PRICE: $435.00

HIGH VOLTAGE POWER SUPPLIES

Fluke high voltage power supplies have become the standard of the industry where quality and reliability are essential. They provide unexcelled performance through sound electrical and mechanical design. Voltages from 0-10,000 and from10,000 to 30,000 are available with current capabilities from 0-50 ma. All instruments incorporate over-current protection circuits.

MODEL	VOLTAGE	CURRENT (ma)	REGULATION LINE	REGULATION LOAD	STABILITY (%) PER HR.	STABILITY (%) PER DAY	CALIBRATION ACCURACY (% of Output)	MAX. RIPPLE RMS	RESOLUTION	PRICE
412B	0-2100V	0-30	0.001	0.001	0.005	0.02	0.25	500 uv	5 mv	$ 410.00
415B	0-3111V	0-30	0.0005	0.0005	0.002	0.01	0.25	100 uv	5 mv	$ 575.00
408B	0-6000V	0-20	0.001	0.001	0.005	0.02	0.25	1 mv	5 mv	$ 700.00
410B	0-10, 000V	0-10	0.001	0.001	0.005	0.02	0.25	1 mv	5 mv	$ 975.00
430A	10KV-30.22KV	0-10	0.005	0.01	0.005	0.03	0.25	5 mv	100 mv	$3940.00

GENERAL PURPOSE POWER SUPPLY- MODEL 407D

VOLTAGE:
0-555V

REGULATION:
Line – 0.005%
Load – 0.01%

CURRENT:
0-300 ma

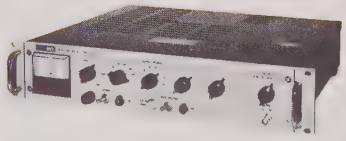
STABILITY:
Per hour – 0.01%
Per day – 0.05%

CALIBRATION ACCURACY:
0.5%

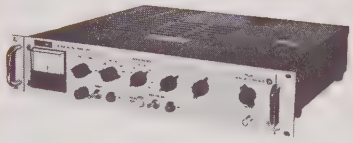
MAX. RIPPLE RMS:
500 uv

RESOLUTION:
2 mv

PRICE:
Cabinet Model (407D) – $450.00
Rack Model (407DR) – $470.00



Model 415B



Model 412B

RATIO MEASUREMENT DEVICES

Fluke provides Kelvin-Varley dividers, reference dividers and lead compensators for use in calibration consoles and ratio measuring systems. Each unit meets the most exacting requirements of the standards laboratory.

KELVIN-VARLEY DIVIDERS

MODEL	INPUT RESISTANCE	LINEARITY	RESOLUTION	MAX. INPUT	VOLTAGE MAX. PWR.	TC OF LINEARITY	PRICE
720A	100k ohm ±0.005% at 1.0 input 110k ohm ±0.005% at 1.1 input	±.1 ppm at dial setting of 0.1 to 1.1	0.1 ppm	1100V	11 watts	±0.1 ppm of input/°C	$1495.00
725A	440k ohm ±0.2% at 1.1 input	±5 ppm at dial setting of 0.1 to 1.1	1 ppm	1100V	2.7 watts	±1 ppm/°C	$ 390.00

REFERENCE VOLTAGE DIVIDER–MODEL 750A

INPUT VOLTAGES	OUTPUT VOLTAGES	DIVIDER CURRENT	TC OF OUTPUT	ACCURACY	STABILITY	PRICE
1.1, 5, 10, 50, 100, 500, 1000, 1100V DC	0.1, 0.5, 1, 1.1, 5, 10, 50, 100, 500, 1000, 1100V DC	1 ma	±1 ppm/°C over operating range	±0.001%	±0.001% per year	$1195.00

LEAD COMPENSATOR–MODEL 721A

4000:1 Max. Ratio Resistance, 0.1 milliohms resolution, 1500 Max. Divider Voltage, Price $295.00

DC CALIBRATION SYSTEMS

The 7100 series DC voltage and ratio calibration systems offer the utmost in accuracy and flexibility. Many combinations and variations are possible, all utilizing off-the-shelf standard Fluke instruments. The 7100 systems may be completely tailored to your individual calibration and measurement applications. Typical applications are calibration of differential voltmeters, digital voltmeters, voltage dividers, reference power supplies, laboratory potentiometers and many more.

THERMAL TRANSFER STANDARD–MODEL 540B

For ±0.01% RMS AC transfer measurements without calibration curves or correction tables, Fluke offers the all solid-state Model 540B AC/DC Thermal Transfer Standard. Thermocouple burnout is virtually eliminated by a unique protection circuit. In addition a search circuit provides visual indication of the percent of rated input. DC input to the unit is conveniently reversed via front panel switch, and DC turnover is held to less than 0.01%.

VOLTAGE RANGE: 0.5 to 1000V in 14 ranges
GALVANOMETER RESOLUTION: 0.0012% of input/scale div. at rated input
ACCURACY (% OF INPUT)

RANGE	FREQUENCY	AC/DC DIFFERENCE
All except 1000V	5 Hz-50 kHz	±0.01%
1000V	5 Hz-20 kHz	±0.02%
1000V	20 kHz-50 kHz	±0.04%
0.5 thru 10V	50 kHz-1 MHz	±0.1%

PRICE: $1045.00 (RECHARGEABLE BATTERIES INCLUDED)

CURRENT TRANSFER ACCESSORIES

Available as accessories for the Model 540B are Thermal Converters (A55), Current Shunts (A40), a Current Transfer Switch (A45), Coaxial Cable Kits (A55-110), and Storage Cases (C41 and C55). See your local representative or contact the John Fluke Mfg. Co., Inc. for more information.

ELECTRONIC GALVANOMETER–MODEL 841A

Unique design, features fast response, virtual immunity to overload damage, battery or AC operation and operation in any position.

FULL SCALE RANGES:

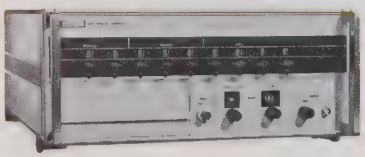
841A
±30 nanoamperes (2 na/scale div.)
±300 nanoamperes (20 na/scale div.)
±3 microamperes (200 na/scale div.)

841B
±100 nanoamperes (5 na/scale div.)
±1 microampere (50 na/scale div.)
±10 microamperes (500 na/scale div.)

INPUT RESISTANCE:
841A—180 ohms
841B—18 ohms

PRICE: $295.00

TIME AND FREQUENCY



FREQUENCY SYNTHESIZER–MODEL 644 SERIES

The all solid state 644 Series Frequency Synthesizers cover the frequency range of 0 to 40 MHz with 3 instruments. The Model 644 provides DC to 40 MHz; the 633 from DC to 11 MHz and the 622 from DC to 2 MHz. All instruments are of modular construction and have the same characteristics of 90 db spectral purity, low phase noise and low noise floor. In addition, all have sweep and search capabilities and can be remotely programmed.

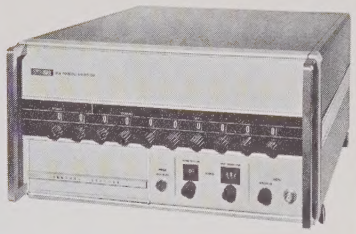
MODEL	FREQUENCY RANGE	FREQUENCY INCREMENTS	FREQUENCY STABILITY AND ACCURACY	PRICE
644A	DC to 40 MHz	0.1 Hz	1 part in 10^8 per day	$10,990.00
633A	DC to 11 MHz	0.1 Hz	1 part in 10^8 per day	$ 7,790.00
622A	DC to 2 MHz	0.1 Hz	1 part in 10^8 per day	$ 7,190.00

NEW-NEW-NEW

FREQUENCY SYNTHESIZER–MODEL 645A

The new Fluke Model 645A Frequency Synthesizer covers the frequency range from DC to 50 MHz in .01 Hz step increments. The spectral purity of this new instrument is at an all time high. All non-harmonically related spurious signals are at least 100 db below the fundamental. The signal-to-phase-noise ratio is also greatly improved. The 645A contains all of the versatile features of the 600 Series family such as, high speed remote programming, internal sweep generator, and modular construction suitable for many varieties of special versions. In addition, the variety of standard options allows tailoring the 645A to most applications, at a bare minimum cost to the customer. The 645A embodies all of the latest state-of-the-art improvements in synthesizer design and packaging to achieve a new standard of performance.

FREQUENCY RANGE	FREQUENCY INCREMENTS	SPURIOUS	FREQUENCY STABILITY AND ACCURACY	SIGNAL-TO-PHASE NOISE RATIO	PRICE
DC to 50 MHz	.01 Hz	All non-harmonically related spurious signals are at least 100 db below the fundamental	1 part in 10^8 per day	Greater than 63 db in a 30 Hz band centered on the carrier but excluding a 1 Hz band centered on the carrier	$13,500.00



FREQUENCY COMPARATOR–MODEL 103A

The Model 103A now makes possible the comparison of test and reference frequencies from 100 kHz to 1 MHz in 100 kHz steps and from 1 MHz to 5 MHz in 1 MHz steps. Output may be read directly on external frequency counter, front panel meters and/or output recorder. Quadrature outputs are available for display on an oscilloscope or XY recorder. Price $1995.00.

FREQUENCY DISTRIBUTION AMPLIFIER-MODEL 203A

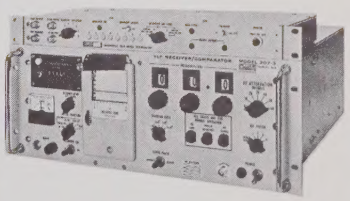
The Model 203A is a multi-channel distribution amplifier that features high stability, free from harmonics and spurious outputs and high inter-channel isolation. These amplifiers are being widely used for distribution of standard frequencies in laboratories, communication installations and industrial facilities. Price $1395.00.

VLF RECEIVER/COMPARATOR–MODEL 207-1

The Model 207-1 is a coherent VLF tracking receiver for calibration of laboratory and communications center frequency standards. Frequency coverage is from 8.0 to 31.9 kHz in steps of 100 Hz with an additional channel at 60 kHz. The instrument is all solid-state and employs a multitude of integrated circuits. Multi-channel capability plus high sensitivity assures round-the-world reception of VLF signals for frequency standardization. Price $2995.00.

OMEGA COMMUTATOR–MODEL 291A

The Omega System of global navigation utilizes a network of highly stable transmitters operating in the VLF spectrum. The Model 291A Omega Commutator is designed to permit selected use of these ultra-stable transmissions for frequency comparison in the 207 series VLF Receiver/Comparators. Price $495.00.



VAW® METER–MODEL 102

The Model 102 Vaw® Meter measures voltage, current, and power over a wide frequency range. It has a maximum true power sensitivity of 225 microwatts and will measure up to 18 kilowatts over the frequency range of 20 Hz to 100 kHz. Cabinet model, $760.00, shunts $30.00 each.

GENERAL INFORMATION

Of necessity information and specifications contained in this brochure are abbreviated. Detailed technical data sheets will be furnished immediately upon request from the Fluke engineering representative in your area, or directly from the factory.

Orders should be made out to John Fluke Mfg. Co., Inc., sent in care of your local Fluke representative or directly to P.O. Box 7428, Seattle, Washington 98133.

U.S. and Canadian terms are 30 days net.

Prices are F.O.B. factory, Mountlake Terrace, Washington, unless otherwise specified. All prices are U.S. funds and are subject to change without notice.

All Fluke instruments are warranted against defective materials and workmanship for one year. All power transformers are warranted for the life of the instrument. Tubes and lamps are considered expendable components and are warranted for 90 days.

* * * * * *

Fluke decade potentiometers and rheostats deliver accuracies and stability comparable to Fluke Instruments.

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